InGaAsP/InP OPTOELECTRONIC INTEGRATED DEVICES AND CIRCUITS FOR OPTICAL SIGNAL PROCESSINGS

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ABSTRACT

The integrated optoelectronics based on InGaAsP/InP materials system are studied for application to optical signal processings. The InGaAsP/InP system is very important for long-wavelength optical fiber communications. Generation, detection, and computing for optical signals are required to achieve optical signal processings. In this study, three devices corresponding to optical signal generation, detection, and computing are developed. Both the fabrication of integrated structures and the characterization of fabricated devices are concerned.

Process technologies for the InGaAsP/InP materials system are described first. They are epitaxial growth, insulator film deposition, etching, dopant diffusion, and metallization. Especially for the etching and the metallization, such new technologies as the reactive ion etching (RIE) using a mixture of Br_2 and Ar gases, and the transmission line model (TLM) method using a new contact arrangement are proposed and utilized.

The integration of a laser diode and a passive waveguide is studied for optical signal generation. Two new integrated structures, a self-aligned integrate loaded (SAIL) guide and a passive/active loaded (PAL) guide, are proposed. Three structures including these two and a bundle-integrated-guide (BIG) are fabricated. The guiding loss of the waveguide and the coupling efficiency between the laser and the waveguide are evaluated for these three structures. The SAIL guide is also applied to the integrated passive cavity (IPC) laser consisting of an active cavity and a long passive cavity. It exhibits stable single longitudinal mode oscillation with a narrow spectral linewidth.

The monolithic photoreceiver incorporating a photodiode and a preamplifier is developed for optical signal detection. The photoreceiver consisting of a pin photodiode, four junction field-effect transistors (FET's), four level shift diodes, and a feedback resistor is successfully designed and fabricated. The bandwidth is measured with respect to dissipation current for the three types of photoreceivers which are distinguished by the gate length and the feedback resistance. The experimental results are

well explained by theoretical considerations, and coincide with the results of computer circuit simulation. Transmission characteristics are measured to evaluate the sensitivity. It is limited by the 1/f noise of the front-end FET and improved by increasing the feedback resistance.

The photonic parallel memory (PPM) which is an array of optoelectronic bistable switches is proposed and fabricated for processing optical signals. The switch consists of a heterojunction phototransistor (HPT) and a light-emitting diode (LED), and the switching and bistable operation are caused by the optical positive feedback from the LED to the HPT. In addition to the electrically erased PPM having only switches, an optically erasable PPM is also demonstrated. The optical reset function is attained by an additional HPT connected to the switch electrically in parallel. The memory operation of the PPM with functions of optical write-in, read-out, and erasing is demonstrated.

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TABLE OF CONTENTS

ABSTRACT i

ACKNOWLEDGEMENTS iii

I. INTRODUCTION 1

References 6

II. PROCESS TECHNOLOGIES FOR InGaAsP/InP MATERIALS 10

2-1. Introduction 10
2-2. Epitaxial Growth 10
2-2-1. Liquid-phase epitaxy 10
2-2-2. Organometallic vapor-phase epitaxy 12
2-3. Insulator Film Deposition 13
2-4. Etching 15
2-4-1. Wet chemical etching 15
2-4-2. Reactive ion etching 16
2-5. Dopant Diffusion 19
2-6. Metallization 20
2-7. Summary 24
References 25

III. INTEGRATION OF A LASER DIODE AND A PASSIVE WAVEGUIDE 28
— INTEGRATED PASSIVE CAVITY (IPC) LASER —

3-1. Introduction 28
3-2. Integrated Device Structures 28
3-3. Fabrication 31
3-4. Characteristics 34
3-4-1. Threshold current 34
3-4-2. Longitudinal mode 38
3-4-3. Spectral linewidth 40
3-5. Discussion 42
3-5-1. Coupling efficiency and guiding loss 42

3-5-2. Analysis for longitudinal mode 44
3-6. Summary 45
References 47

IV. INTEGRATION OF A PIN PHOTODIODE AND AN AMPLIFIER CIRCUIT — MONOLITHIC PHOTORECEIVER — 49

4-1. Introduction 49
4-2. Integrated Circuit Design 49
4-2-1. Device structures 49
4-2-2. DC bias point 51
4-2-3. Frequency response 55
4-3. Fabrication 57
4-4. Characteristics of Composite Devices 59
4-4-1. General characteristics of FET's 59
4-4-2. Output resistance of FET's 62
4-4-3. Characteristics of PD's 64
4-5. Circuit Characteristics 65
4-5-1. Circuit operation 65
4-5-2. Dissipation current and bandwidth 67
4-5-3. Transmission characteristics 71
4-6. Photoreceiver with Self-Aligned FET's 72
4-6-1. Device structures 72
4-6-2. Fabrication 74
4-6-3. Characteristics of FET's 75
4-6-4. Circuit characteristics 77
4-7. Approach to a photoreceiver grown by OMVPE 78
4-7-1. Device structures 78
4-7-2. PD with a window layer 79
4-7-3. Self-aligned FET 79
4-8. Discussion 81
4-8-1. Analysis for bandwidth 81
4-8-2. Analysis for sensitivity 82
4-9. Summary 84
References 85

V. INTEGRATION OF OPTOELECTRONIC BISTABLE SWITCHES 88
— PHOTONIC PARALLEL MEMORY (PPM) —

5-1. Introduction 88
5-2. Integrated Device Structures 89
5-2-1. Operation principle 89
5-2-2. Electrically erased PPM 90
5-2-3. Optically erasable PPM 91
5-3. Fabrication 92
5-4. Characteristics of EE-PPM's 95
5-4-1. Array operation 95
5-4-2. Static characteristics 96
5-4-3. Switching speed 99
5-5. Characteristics of OE-PPM's 101
5-5-1. Array operation 101
5-5-2. Static characteristics 102
5-5-3. Switching speed 105
5-6. Proposals for application of the PPM 105
5-6-1. Crossbar switchboard 105
5-6-2. Free-space interchip connections 106
5-6-3. Optical parallel logic gates 107
5-7. Discussion 109
5-7-1. Analysis for dissipation current 109
5-7-2. Relation of input and output power 110
5-7-3. Improvement for switching speed 110
5-8. Summary 111
References 112

VI. CONCLUSIONS 115

ADDENDUM 120

List of Publications 120
List of Presentations 122

I. INTRODUCTION

The remarkable progress of electronics has been attained through the integration technologies of Si electronic devices. Optoelectronic devices based on alloy and compound semiconductors, such as AlGaAs/GaAs and InGaAsP/InP, are now on the way to integration as electronic devices have been evolved from discrete devices into integrated circuits (IC's). It is the natural trend of development in optoelectronics to pursue the integration of optoelectronic devices.

In general, the integration technologies of optical or optoelectronic devices are classified into two categories. One is "integrated optics" or an "optical IC" which is aimed at the integration of different kinds of optical devices. The other is an "optoelectronic integrated circuit" (OEIC) in which optoelectronic devices are integrated with electronic circuits. The OEIC's are fabricated only on semiconductor substrates, while dielectric and semiconductor substrates are used for optical IC's.

The dielectric optical IC's consist of the optical devices which do not perform conversions between photons and electrons. On the other hand, some semiconductor optical IC's include optoelectronic devices converting electrons to photons or vice versa. From the viewpoint of this thesis standing on optoelectronics, the semiconductor optical IC's incorporating optoelectronic devices are only taken into consideration among optical IC's. The field including both this kind of optical IC's and the OEIC's can be termed as "integrated optoelectronics".

In this thesis, the third category of integration is added to the integrated optoelectronics. It is an "optoelectronic integrated device" (OEID) proposed by A. Sasaki [1]. The OEID is distinguished from the OEIC as follows: In the OEIC, optoelectronic devices and electronic devices are integrated monolithically onto a semiconductor substrate, and they are connected with electrically conducting elements. The OEID is the monolithic integration of devices onto a semiconductor substrate, with no conducting elements being used for the connection among them.

The basic idea of the integrated optics was first proposed by S.E. Miller in 1969 [2]. It is a proposal for a miniature form of laser beam circuitry in which a dielectric waveguide is used not only as the means of optical connecting but also as active devices such as a laser, a modulator, and a directional coupler. The purpose of the integration is to isolate the laser circuit assembly from thermal, mechanical, and acoustic ambient changes through small overall size, and thus reliability and economy are expected as ultimate result.

The basic components for Miller's IC are a "passive" waveguide transparent for signal light and a laser with an "active" waveguide. The integrated structures of a laser and a passive waveguide were fabricated successively in 1974-75 [3-6]. Though they were exhibition of integration itself, one of them demonstrated the modulation of laser output using a passive waveguide [3]. Afterward, a passive waveguide was used as a wavelength multiplexer combined with six distributed-feedback (DFB) lasers [7], and one of two lasers coupled through a passive waveguide was used as a detector or an amplifier [8,9].

All of the integrated structures described above were fabricated with the AlGaAs/GaAs materials system. However, it is required to use the InGaAsP/InP materials system for long-wavelength (1.3 - 1.6 μm) optical fiber communications. The integration of an InGaAsP/InP laser and a passive waveguide was first demonstrated in 1980-82 [10,11], in which a passive waveguide was used as a distributed Bragg reflector [10] and two lasers coupled through a passive waveguide were used as optically coupled lasers, a laser with a photodiode, or a resonant optical amplifier [11]. In the same period, optical switch, which is thought to be another important active device in the optical IC, was fabricated using InGaAsP/InP [12,13], and the integration of DFB lasers and an optical switch was also demonstrated [14].

On the other hand, A. Yariv proposed the integration of optoelectronic and electronic devices in 1972 [15]. The expected merits of integration were high reliability, low cost, and small size as well as high-speed operation because of the reduction of

parasitic capacitance and inductance between optoelectronic and electronic devices. Yariv's proposal was embodied to be a real IC by C.P. Lee et al. in 1978 [16]. It was the first OEIC on a GaAs substrate, in which a laser diode and a Gunn oscillator were integrated. The OEIC on an InP substrate was first fabricated by R.F. Leheny et al. in 1980 [17]. It was a receiver OEIC consisting of a pin photodiode and a junction field-effect transistor.

Though the concept of the OEIC was born in USA and the first OEIC was fabricated also in USA, the development of OEIC's has been led by companies in Japan after 1980. This is because the OEIC was recognized as a key device in the National Research and Development Project entitled "Optical Measurement and Control Systems" which is started in 1979 by the Ministry of International Trade and Industry (MITI) in Japan. In the project, development of GaAs-based OEIC's was mainly promoted [18,19], while InP-based OEIC's were developed in parallel but independently of the project [20-23]. As a result, the basic technologies for integrating a laser diode or a photodetector with electronic circuits for both material systems were fairly well developed until 1986.

The recent research areas of the integrated optoelectronics are thought to be classified into three categories summarized in Table 1-1. This classification has been proposed by the author [24]. In this table, "OEIC" is the successor of the prototype OEIC. It incorporates a single optoelectronic device and a large electronic circuit. The current interest in the OEIC is low cost and high-speed operation. The former will make the OEIC to be a key device for fiber-optic subscriber systems and the latter is important to apply the OEIC to large capacity optical fiber transmissions.

The second category is the semiconductor optical IC incorporating optoelectronic devices, which is recently called as a "photonic IC" (PIC) [25]. The PIC incorporates different kinds of optical and optoelectronic devices connected with optical waveguides. Although it has not been realized yet, the most attractive application of the PIC is an integrated coherent optical

receiver incorporating a frequency-stabilized DFB laser, a 3-dB coupler, a balanced receiver, and surrounding circuits [26].

In the OEIC, optoelectronic and electronic devices are connected with conducting wires, and they form the circuit. In the PIC, those devices are connected with optical waveguides, and they form the circuit. However, optoelectronic devices can be connected or integrated directly, and they form just like a new device. This is the OEID classified in the third category. The OEID creates new functions such as optical amplification, optical bistability, and optical switching which are hard to be observed in individual devices [27]. The OEID has the advantage to be integrated in a large scale two-dimensional array. In the array, optical signals are processed independently by each constituent and conducting elements are used only for power supply.

From another viewpoint, the OEIC, the PIC, and the OEID are optically one, two, and three-dimensional devices, respectively. The optoelectronic device in the OEIC is usually coupled to an

Table 1-1 Classification of recent research areas in the integrated optoelectronics (OEIC: optoelectronic integrated circuit, PIC: photonic integrated circuit, OEID: optoelectronic integrated device, TDM: time division multiplexing, and WDM: wavelength division multiplexing).

	OEIC	PIC	OEID
CONFIGURATION			
OPTICAL DIMENSION	1D (FIBER)	2D (WAVEGUIDE)	3D (FREE SPACE)
ADVANTAGES	ULTRA-HIGH SPEED SMALL SIZE & LOW COST	MULTI-FUNCTION EFFICIENT COUPLING	PARALLEL TRANSMISSION PARALLEL PROCESSING
APPLICATIONS	TDM TRANSMISSION SUBSCRIBER SYSTEM	COHERENT RECEIVER WDM TRANSMISSION	INTERCONNECTION DIGITAL COMPUTING

optical fiber which guides the optical signal one-dimensionally. In the PIC, the optical and optoelectronic devices are connected with optical waveguides laid two-dimensionally on the substrate plane. The OEID can be arranged in a two-dimensional array, and optical signals are transmitted three-dimensionally in the free space.

As described above, the OEIC, the PIC, and the OEID are distinguished by their configurations, optical dimensions, advantages, and applications. However, the process technologies for fabricating them are almost common. Furthermore, the classification is valid only for the current devices. In the future, electronic circuits will be integrated also in the PIC, and a two dimensional array of OEIC's will be developed. The former is the combination of OEIC and PIC, and the latter is that of OEIC and OEID. Any combination among the OEIC, the PIC, and the OEID will be constructed if the problems in fabrication are solved. In other words, all of the OEIC, the PIC, and the OEID are in the field of integrated optoelectronics based on the same process technologies and will be unified into a single category in the future.

The historical background, the current status, and the future trend of the integrated optoelectronics have been reviewed and discussed. As described in them, the InGaAsP/InP materials system is very important for applications to long-wavelength optical fiber communications. The purpose of this study is to advance the InP-based integrated optoelectronics through upgrading the process technologies for the InGaAsP/InP materials. In this study, three types of devices are developed for optical signal processings. Generation, detection, and computing for optical signals are required to achieve optical signal processings. The three devices correspond to optical signal generation, detection, and computing. In addition, they are typical examples of the PIC, the OEIC, and the OEID.

The thesis is composed of six chapters as follows: In Chapter II, the process technologies for InGaAsP/InP materials are described. They are epitaxial growth, insulator film deposition,

etching, dopant diffusion, and metallization. The process technologies are advanced through the development of devices presented in the following chapters. The devices are successfully fabricated owing to the process technologies developed herein.

In Chapter III, the integration of a laser diode and a passive waveguide is presented. It is the integration in optical signal generation, and is the basic combinations for constructing PIC's. Three integrated structures are fabricated and characterized as a laser diode with a monolithically-integrated external cavity. The guiding loss of the waveguide and the coupling efficiency between the laser and the waveguide are evaluated for these structures.

In Chapter IV, a monolithic photoreceiver incorporating a pin photodiode and an amplifier circuit is demonstrated. It is a typical OEIC for optical signal detection. The photoreceiver incorporating a pin photodiode, four junction field-effect transistors, four level shift diodes, and a feedback resistor is successfully designed and fabricated. The frequency response and the sensitivity of the photoreceiver are measured, and the limitation factors for them are analyzed.

In chapter V, a two-dimensional array of optoelectronic bistable switches is demonstrated. It is the OEID based on the new concept proposed in this study, that is, a large scale integration of optoelectronic devices with an identical structure. This array has potential application to optical interconnections and optical digital computing.

In Chapter VI, major and important results obtained through this study are summarized.

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II. PROCESS TECHNOLOGIES FOR InGaAsP/InP MATERIALS

2-1. Introduction

The fabrication steps of InGaAsP/InP integrated devices are basically the same as those of Si or GaAs IC's. Epitaxial growth of semiconductor crystals, deposition of insulator films, photolithography, processing for crystals such as etching and dopant diffusion, and metallization are repeated to accomplish the device structures. However, the epitaxial growth takes more important part in integrated optoelectronics than in the fabrication of Si IC's since it constructs heterostructures being essential in optoelectronic devices. In regard to the processing for crystals, the etchants and the dopants for InP or InGaAsP are different from those for Si or GaAs, and metals for ohmic contacts are also different. Deposition methods of insulator films used in the Si process can be applied to InP though more carefulness is required for deposition conditions because InP is damaged more easily than Si or GaAs by heat treatment or plasma exposure.

In this chapter, the process technologies for the InGaAsP/ InP materials system, such as epitaxial growth, insulator film deposition, etching, dopant diffusion, and metallization, are described in detail. They are advanced through the development of devices presented in Chapters III, IV, and V. The devices are successfully fabricated owing to the process technologies developed herein. Thus the process technologies described in this chapter and the device technologies in Chapters III - V are closely related and support each other just like two wheels of a cart.

2-2. Epitaxial Growth

2-2-1. Liquid-phase epitaxy

The methods for epitaxial growth of III - V semiconductor materials are generally classified into liquid-phase epitaxy (LPE), halide and hydride vapor-phase epitaxy (VPE), organometallic vapor-phase epitaxy (OMVPE), and molecular beam epitaxy (MBE). Among them, LPE is the most established technology. High-quality epitaxial layers can easily be obtained by LPE though the growth

of very thin (< 0.1 μm) layers and the precise control of layer thickness are difficult. LPE has been used to grow epitaxial layers for all the devices demonstrated in this thesis except for the monolithic photoreceiver with an improved structure.

The apparatus for LPE used in this study is a common slide type [1]. A graphite boat with eight bins is loaded in a three-zone furnace with a PID-temperature controller and a high-speed boat loader. The supercooling technique [2,3] was used for the growth of InP, InGaAs, and thick (> 1 μm) InGaAsP layers with a cooling rate of about 0.7 °C/min, while thin (< 0.5 μm) InGaAsP layers were grown by the two-phase solution technique [2,4]. The soaking was done at a temperature of 670 °C for 90 min and the growth was started at about 635 °C. The exact growth temperature and the liquidus composition for each layer have been determined corresponding to the solidus composition and the layer thickness. Typical growth conditions for InP, InGaAsP, and InGaAs layers are summarized in Table 2-1. An example of a cross-sectional scanning electron microscope (SEM) photograph of InGaAsP and InP layers grown by LPE is shown in Fig. 2-1.

Table 2-1 Typical conditions of LPE growth for InP, InGaAsP, and InGaAs layers.

SOLIDUS COMPOSITION	THICKNESS (μm)	GROWTH METHOD	TEMPERATURE(°C)	TIME (SEC)	LIQUIDUS COMPOSITION x^{ℓ}_{Ga}	x^{ℓ}_{As}	x^{ℓ}_{P}
InP	0.9	S.C.	635.0	200	0	0	0.65
InP	0.9	S.C.	630.2	100	0	0	0.63
InGaAsP (λ_g = 1.1 μm)	1.2	S.C.	632.0	40	0.39	3.00	0.40
InGaAsP (λ_g = 1.3 μm)	0.3	T.P.	635.0	7	0.97	4.90	>0.19
InGaAsP (λ_g = 1.3 μm)	0.3	T.P.	630.2	10	0.90	4.70	>0.19
InGaAs	2.0	S.C.	630.0	22	2.40	5.44	0

λ_g: Bandgap wavelength, S.C.: Supercooling, T.P.: Two-phase

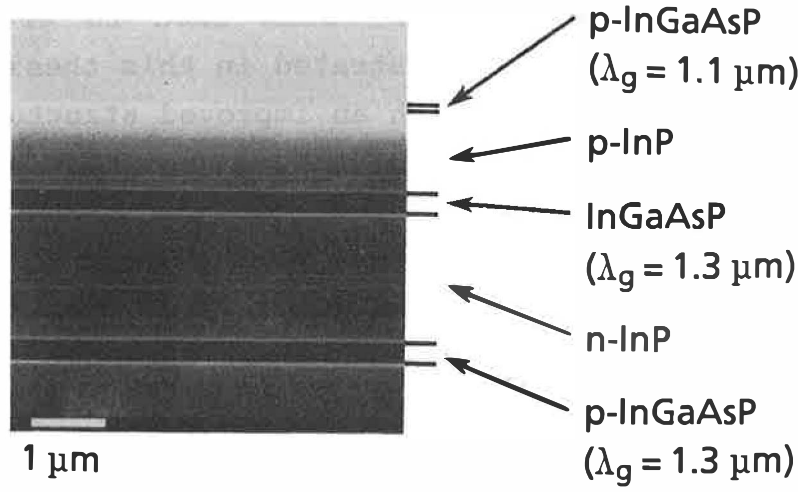

Fig. 2-1 Cross-sectional SEM photograph of InGaAsP and InP multilayers grown by LPE.

2-2-2. Organometallic vapor-phase epitaxy

Compared with LPE, OMVPE has advantages in controllability and uniformity of grown-layer thickness which enable one to grow very thin layers. Furthermore, it has two additional advantages which are utilized in growth of the epitaxial layers for the monolithic photoreceiver. The first is the growth of InP on InGaAs. It is usually impossible to grow this layer structure by using LPE

Table 2-2 Typical conditions of OMVPE growth for InP and InGaAsP layers.

SOLIDUS COMPOSITION	THICKNESS (μm)	TEMPERATURE(°C)	PRESSURE (Torr)	TIME (min)	FLOW RATE (mol/min) TEIn	TEGa	AsH_3	PH_3
InP	0.5	600	150	17	2.14×10^{-5}	0	0	1.12×10^{-3}
InGaAsP (λ_g = 1.1 μm)	0.5	670	150	19	1.19×10^{-5}	2.14×10^{-6}	8.93×10^{-5}	1.38×10^{-3}

λ_g: Bandgap wavelength

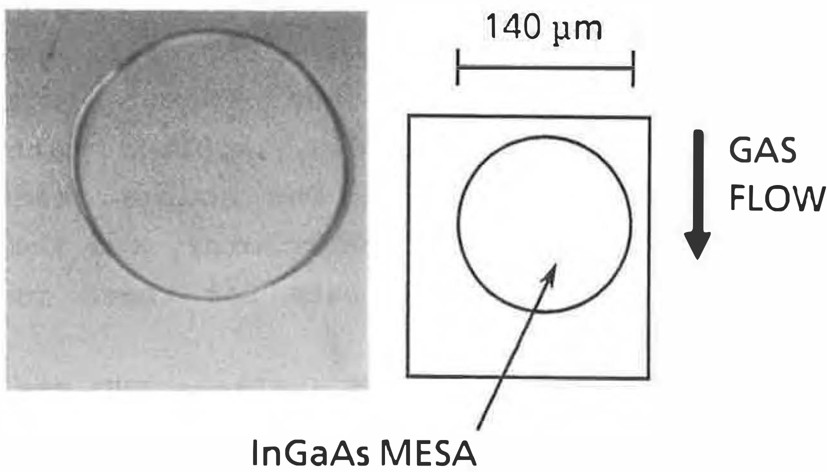

Fig. 2-2 Photomicrograph of an InP layer grown by OMVPE on the InP substrate with an InGaAs mesa.

since InGaAs is dissolved in the In melt supersaturated with P. The second is the growth on the substrate with mesa-shape structures which usually cause residuals of the In melt after wipe-off during the LPE growth.

The apparatus for OMVPE used in this study is a low pressure OMVPE system composed of a fast switching manifold with low dead volume and a horizontal quartz reactor which contains a graphite susceptor [5]. The susceptor is heated inductively and has a tilted angle of 15° against gas flow. Typical growth conditions for InP and InGaAsP layers are summarized in Table 2-2. Triethylindium (TEIn), triethylgallium (TEGa), AsH_3, and PH_3 are used as source materials and H_2 as a carrier gas with a total flow of 6500 cc/min. A photomicrograph of an InP layer grown by OMVPE on the InP substrate with InGaAs mesas is shown in Fig. 2-2. A smooth and uniform layer is grown both on tops and on side walls of the mesas.

2-3. Insulator Film Deposition

Two kinds of insulator films have been used in fabrication process. They are SiO_2 deposited with chemical vapor deposition (CVD) and SiN_x with plasma CVD. The latter film has advantages of

good step-coverage and relatively low deposition temperature though high-temperature heat cycle after deposition often generates cracks in it. To prevent this, the SiO_2 film was overlaid on SiN_x in some cases. The SiO_2 film was deposited with an atmospheric-pressure CVD system (AMS2600, Applied Materials). The deposition temperature was 420 °C. The source gases were SiH_4 (N_2-base, 5%, 680 cc/min) and O_2 (303 cc/min), and the carrier gas was N_2 (62 ℓ/min). The deposition rate for these conditions was 500 Å/min.

The SiN_x film was deposited with a plasma CVD system (PED301, Anelva). The source gases were SiH_4 (Ar-base, 5%, 70 cc/min) and NH_3 (10 cc/min). The gas pressure and the plasma power were 300 mTorr and 200 W, respectively. The deposition temperature were varied within the range from 270 °C to 350 °C depending on the use of the film. Below 270 °C, bubbles are formed in the film which is thought to be caused by insufficient decomposition of source gases. Above 350 °C, the coarse and opaque film is deposited. This phenomenon is enhanced in deposition of the film on InGaAsP/InP epitaxial layers compared with that on Si and InP substrates. The deposition rate was approximately 550 Å/min which did not strongly depend on the deposition temperature.

In fabrication steps of the devices, insulator films are used as an etching mask, a diffusion mask, an underlay for lift-off, and a passivation film. The sort and thickness of films and the deposition temperature of SiN_x for each case are summarized below along with the reasons for choosing them.

(1) Etching mask:

Dual films of lower SiN_x (2000 Å, deposited at 350 °C) and upper SiO_2 (2000 Å), or

a single film of SiN (3000 Å, deposited at 350 °C).

The SiN_x film is more adhesive to InGaAsP/InP crystals and cause less amount of side-etching than SiO_2. Furthermore, SiN_x deposited at higher temperature has higher quality and better adhesiveness. Therefore, SiN_x deposited at the upper-limit temperature was used as a lower film. The upper film of SiO_2 was adopted for fear of pinholes of SiN_x though the single film of

SiN_x caused no problems.

(2) Diffusion mask:

Dual films of lower SiN_x (3000 Å, deposited at 350 °C) and upper SiO_2 (3000 Å).

SiN_x deposited at the upper-limit temperature was used as a lower film owing to the same reason as that for selecting the etching mask. Lateral extraordinary diffusion along the interface between the film and the crystal was observed in case of using SiO_2 as a diffusion mask. The upper film of SiO_2 was adopted to prevent the formation of cracks in the SiN_x film during the diffusion.

(3) Underlay for lift-off:

A single film of SiN_x (3000 or 4000 Å, deposited at 270 - 350 °C).

The underlay for lift-off was used with photoresist on it to form an overhang structure since Au-based metals are difficult to be lifted-off in case of using only photoresist as a stencil. When the film is used as the underlay, quality and adhesiveness of the film is not important, but the amount of side-etching for the film should be controlled. The side-etching of SiN_x can easily be controlled since it is etched with reactive ion etching (RIE) using CF_4, while SiO_2 is usually etched by wet chemical etching.

(4) Passivation film:

A single film of SiN_x (3000 Å, deposited at 270 - 300 °C).

The passivation film is deposited after lift-off of contact metals. Since the contact metals are alloyed with InP above 300 °C, the deposition of passivation film has to be done below this temperature. Furthermore, damages of crystals caused by the deposition should be considered. The deposition of SiN_x with plasma CVD generates damages in crystals to some extent. To avoid this, polyimide was used as a passivation film for some devices.

2-4. Etching

2-4-1. Wet chemical etching

Compared with dry etching, wet chemical etching is not suit-

Table 2-3 Typical preferential etchants and their etching rates for InP, InGaAsP, and InGaAs.

CRYSTAL \ ETCHANT	$HC\ell : H_3PO_4$ (1 : 4 in volume)	$H_2SO_4 : H_2O_2 : H_2O$ (5 : 1 : 1 in volume)	$H_2SO_4 : H_2O_2 : H_2O$ (1 : 1 : 5 in volume)
InP	5000 Å/min	< 100 Å/min	< 50 Å/min
InGaAsP (λ_g=1.1 μm)	~ 0	500 Å/min	200 Å/min
InGaAsP (λ_g=1.3 μm)	~ 0	—	1500 Å/min
InGaAs	~ 0	—	2 μm/min

able for fine patterning due to side-etching. However, it is very useful since InP, InGaAsP, and InGaAs layers can be etched selectively by using preferential etchants. The preferential etchants are indispensable for layer-by-layer etching especially in case of using LPE for epitaxial growth, because thickness of layers are not uniform even within a single wafer. The typical preferential etchants and their etching rates for InP, InGaAsP, and InGaAs are summarized in Table 2-3.

The InP crystal on InGaAsP is etched selectively by HCl solution. The end point of etching is usually judged by observing the surface of the wafer. The foaming continues while InP is etched and stops when the surface of InGaAsP is exposed. The InGaAsP or InGaAs crystal on InP are etched by H_2SO_4 solution. In this case, change of color caused by interference is finished at the end point.

2-4-2. Reactive ion etching

The reactive ion etching (RIE) and reactive ion beam etching (RIBE) are attractive for fine patterning of crystals since vertically etched walls with small amount of side-etching can be ob-

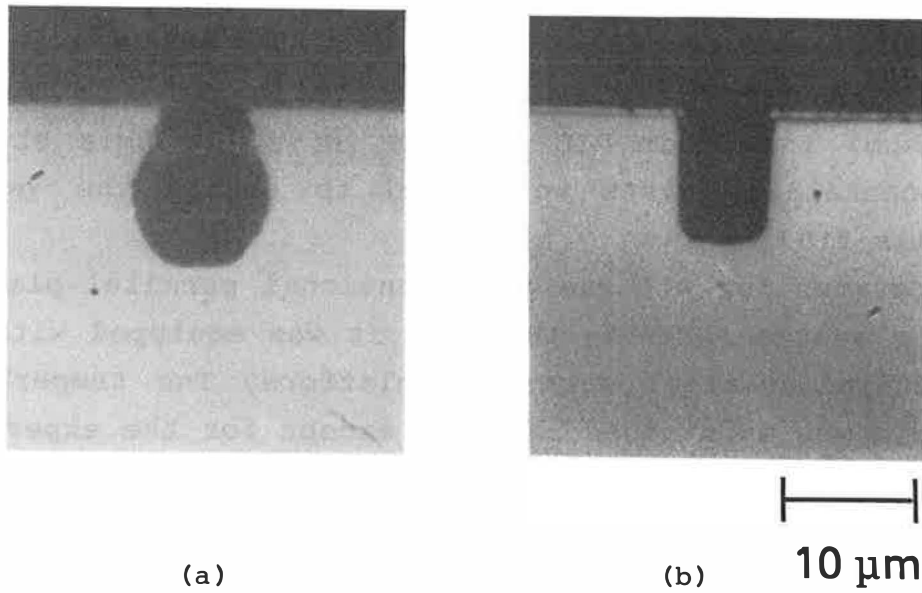

Fig. 2-3 Typical etching profiles of InP wafers using either (a) neat Br_2 or (b) 80% Br_2 and 20% N_2. The etching conditions in (a) are a gas pressure of 17 mTorr, a plasma power density of 0.63 W/cm^2, a substrate temperature of 10 °C, and an etching time of 10 min. Those in (b) are 4 mTorr, 0.63 W/cm^2, 10 °C, and 5 min.

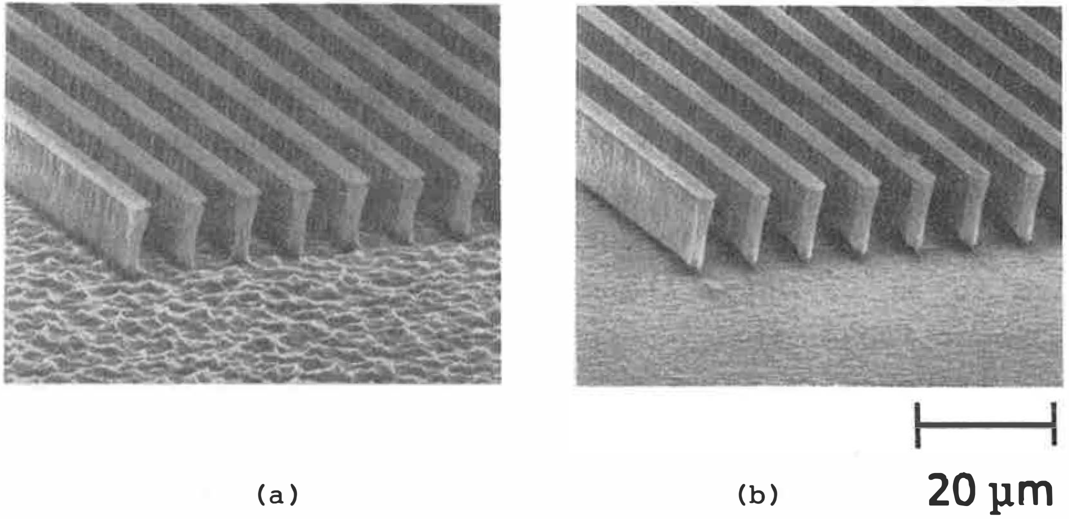

Fig. 2-4 SEM photographs of etched InP wafers using 86% Br_2 and 14% Ar at a substrate temperature of (a) 10 °C or (b) 40 °C. The etching conditions in (a) and (b) are a gas pressure of 4 mTorr, a plasma power density of 0.63 W, and an etching time of 5 min.

tained. Such etching was attained for GaAs by RIE and RIBE with Cl_2-containing gases [6,7]. However, Cl_2 is not a suitable gas for the InGaAsP/InP system since etching rate is very slow (0.05 - 0.2 μm) in either RIE or RIBE [8,9]. In this study, RIE with Br_2-containing gases were used to obtain the vertically etched walls [10].

The apparatus for RIE was a conventional parallel-plate sputter-etching system (DEM451, Varian). It was equipped with a heat or cool stainless-steel substrate platform. The temperature of the platform was maintained at 10 °C except for the experiment in which substrate was heated. The mask for RIE was Ti (4000 Å) formed with electron beam evaporation. Ti is an ideal mask for Br_2-RIE since etching rate of Ti is approximately zero compared with the crystal. The SiN_x (2000 Å) was deposited before evaporation of Ti to prevent reaction between Ti and etched crystal.

When neat Br_2 was used as a etching gas, vertical walls were not obtained for any conditions of gas pressure and plasma power though etching rate of more than 1 μm/min was achieved. The photomicrograph of a typical etching profile using neat Br_2 is shown in Fig. 2-3(a). The etching conditions for Fig. 2-3(a) are a gas pressure of 17 mTorr and a plasma power density of 0.63 W/cm^2. On the other hand, vertical walls shown in Fig. 2-3(b) was obtained by using 80% Br_2 and 20% N_2 with a gas pressure of 4 mTorr and a plasma power density of 0.63 W/cm^2. Further experiments revealed that the smoothness of the etched surface is improved as show in Fig. 2-4 by substituting Ar for N_2 and heating the substrate temperature to 40 °C. Under these conditions, the etching rate for InP is about 1.8 μm/min.

The difference of experimental results between RIE using neat Br_2 and that using a mixture of Br_2 and N_2 or Ar can be explained as follows. In case of using neat Br_2, chemical etching process is dominant. Chemical etching occurs when a chemical reaction takes place on the surface and the resulting products volatilize. It is nondirectional and highly selective for etched materials. On the other hand, the effect of physical etching appears when N_2 or Ar is added to Br_2. Physical etching uses the impact of oncom-

ing ions to sputter material from the surface. It is highly directional (anisotropic) but not very selective. In a mixture of Br_2 and N_2 or Ar, vertical walls are fabricated since chemical etching and physical etching are well balanced.

2-5. Dopant Diffusion

In fabrication of heterostructure devices, dopants are usually added to crystal layers during epitaxial growth. Therefore, dopant diffusion is used only to obtain homojunctions. In this study, the diffusion of Zn is used to form a p-type region of the InGaAs pin photodiode and a gate of the InGaAsP junction field effect transistor (FET), both of which are integrated in the monolithic photoreceiver.

The diffusion of Zn was carried out by using a quartz ampule. The sample wafers were first inserted to the cleaned and baked ampule with the diffusion sources of ZnP_2 and $ZnAs_2$ which are also sources of P and As vapor preventing evaporation of P and As

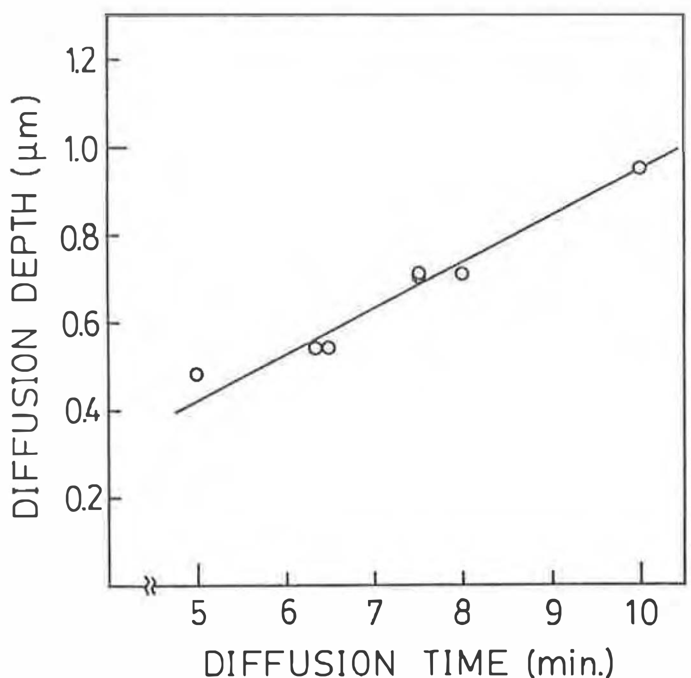

Fig. 2-5 Relation between time and depth for diffusion of Zn into an InGaAsP layer. The diffusion temperature is 500 °C.

from the wafer. The amount of ZnP_2 and $ZnAs_2$ were fixed to be 0.1 mg/cc. Then the ampule was evacuated to a pressure less than 1×10^{-6} Torr and enclosed by fusing the bottom. After enclosing, only the diffusion sources were preheated to remove the oxides on surfaces of them. Finally, the ampule was set to the furnace and heated to 500 °C.

Though the diffusion depth is controlled by diffusion time, the background pressure before diffusion also affects the diffusion depth. When the background pressure is high due to the leakage caused by the failure of enclosing, the diffusion depth becomes shallow or the diffusion is not carried out at all. Taking care of this, the diffusion depth can be controlled precisely by diffusion time as shown in Fig. 2-5. It is a result for diffusion of Zn to InGaAsP ($\lambda_g = 1.1$ µm). Though diffusion depth is proportional to a square root of diffusion time, they are in linear relation in Fig. 2-5. This is because the time necessary to heat up the ampule is included in the diffusion time.

2-6. Metallization

Metallization are usually repeated three times to complete the devices since the ohmic-contact metals for p-type and n-type crystals, and the interconnection metal are different. To obtain ohmic contact for p-InGaAsP and p-InGaAs, Au-Zn (100 Å Zn in 3100 Å Au) or Cr/Pt/Au (500 Å/1000 Å/1500 Å, from lower to upper) was used. For n-InP and n-InGaAsP, Au-Sn (150 Å Sn in 3100 Å Au) was utilized. Au-Zn and Au-Sn are alloyed with the crystals, while Cr/Pt/Au is not alloyed. The alloy contact usually has lower contact resistance than the non-alloy contact though the non-alloy contact should be used when shallow junction is located just beneath the contact. In regard to interconnection metal, Ti/Au (500 Å/0.5-1.0 µm) was used in which Ti plays a role to improve adhesiveness between Au and the insulator films.

To form a Au-Zn contact, Au (100 Å), Zn (100 Å), and Au (3000 Å) were evaporated sequentially. The first thin layer of Au is necessary to improve the adhesiveness of the metals to the crystal for lift-off process which is usually used for patterning

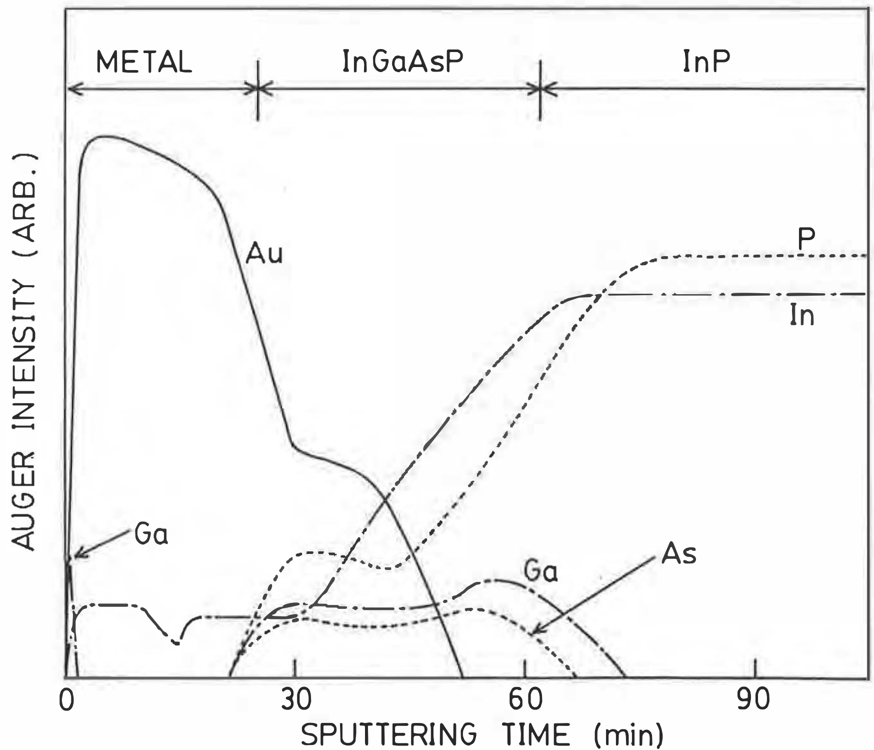

Fig. 2-6 Depth profile of Auger electron spectroscopy for Au-Zn contact on an InGaAsP layer. Au (100 Å), Zn (100 Å), and Au (3000 Å) are evaporated sequentially and alloyed at 420 °C. The InGaAsP layer has a thickness of 0.5 μm.

contact metals. After lift-off, the evaporated metals were annealed at 420 °C for 1 min in H_2 atmosphere. During annealing, Au and the crystal beneath it were alloyed. A depth profile of Auger electron spectroscopy for Au-Zn contact on an InGaAsP layer is shown in Fig. 2-6. The thickness of alloyed layer is about 3000 Å since the InGaAsP layer has a thickness of 0.5 μm. For Au-Sn contacts, Sn (150 Å) was substituted for Zn and annealed with the same conditions as Au-Zn.

The contact resistivity of the formed contact was evaluated by transmission line model (TLM) method. In the conventional TLM method [11-13], rectangular contacts with a length of d and a width of W are arranged on a diffused resistor as shown in Fig. 2-7(a). The number of the contacts are more than three and the distances between the contacts (ℓ) are changed. By plotting

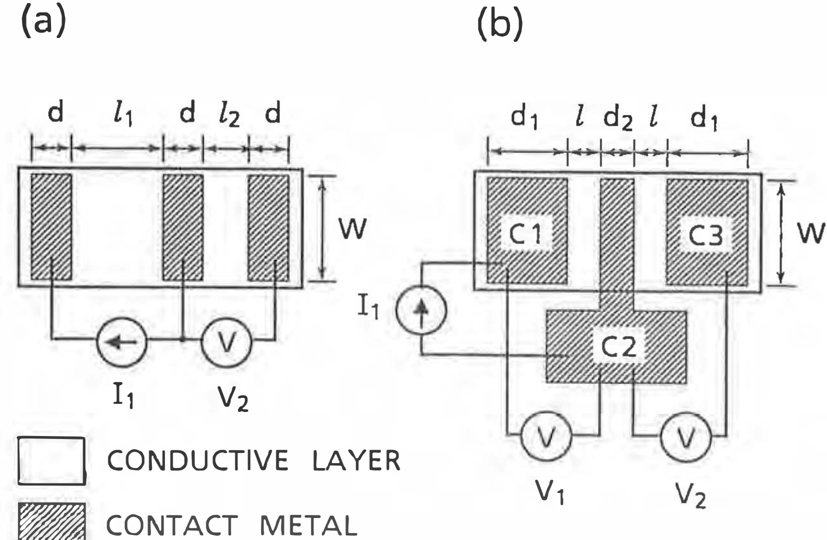

Fig. 2-7 Layout of a thin conductive layer and contact metals: (a) for the conventional TLM method and (b) for a new TLM method proposed in this study.

the values of resistance between the contacts against ℓ, the sheet resistance (R_S) and the contact resistance (R_C) are obtained from the slope and the extrapolated value of the resistance at $\ell = 0$. By assuming the contact resistance of a contact on a thin conductive layer follows the TLM, R_C is given by using R_S and the contact resistivity (ρ_C) as

$$R_C = Z \coth(\alpha d) \qquad (2\text{-}1)$$

where $$\alpha = (R_S / \rho_C)^{\frac{1}{2}} \qquad (2\text{-}2)$$

and $$Z = (R_S \rho_C)^{\frac{1}{2}} / W. \qquad (2\text{-}3)$$

When the contacts are long enough for satisfying $\alpha d > 2$, Eq. (2-1) is simplified to $R_C = Z$. Therefore, ρ_C is obtained from R_C and R_S by using Eq. (2-3).

Though the conventional TLM assumed that the sheet resistance of the conductive layer beneath the contacts (R_{SK}) was the same as that between the contacts (R_{SH}), they have different values

especially in case of alloy contacts. In this case, R_S in Eqs. (2-2) and (2-3) is changed to be R_{SK}, while the R_S obtained from the slope is R_{SH}. To obtain R_{SK}, the modified TLM methods have been proposed [14,15]. One of the modified TLM method [15] utilizes a contact end resistance (R_E) which is defined as V_2/I_1 in Fig. 2-7(a). Using TLM, R_E is given by

$$R_E = Z / \sinh(\alpha d). \qquad (2\text{-}4)$$

By using Eqs. (2-1) - (2-4), ρ_c and R_{SK} are obtained.

In this study, a new TLM method using the contact arrangement shown in Fig. 2-7(b) has been proposed and utilized. Though R_E is measured also in this method, the calculation to obtain α and Z is drastically simplified by adopting a new contact arrangement. For the contacts shown in Fig. 2-7(b), the total contact resistance (R_{CT}) of contacts C1 and C2 is obtained by

$$R_{CT} = V_1/I_1 - (\ell/W) R_{SH} \qquad (2\text{-}5)$$

where R_{SH} is measured by the conventional TLM method. On the other hand, R_{CT} is given by using Eq. (2-1) as

$$R_{CT} = Z\,[\coth(\alpha d_1) + \coth(\alpha d_2)]$$

$$\simeq Z\,[1 + \coth(\alpha d_2)] \quad (\text{in case of } \alpha d_1 > 2) \qquad (2\text{-}6)$$

By solving Eqs. (2-4) and (2-6) for α and Z, the following equations are obtained.

$$\alpha = (1/d_2)\ \ln(R_{CT} / R_E) \qquad (2\text{-}7)$$

$$Z = (1/2)\ (R_{CT} - R_E^2 / R_{CT}) \qquad (2\text{-}8)$$

Furthermore, ρ_c and R_{SK} are obtained by solving Eqs. (2-2) and (2-3) as

$$\rho_c = Z W / \alpha \qquad (2\text{-}9)$$

$$R_{SK} = \alpha Z W \qquad (2\text{-}10)$$

Therefore, ρ_c and R_{SK} are calculated from the measured value of R_{CT} and R_E by using Eqs. (2-7) - (2-10).

The measured values of ρ_c, R_{SK}, and R_{SH} for Au-Zn and Cr/Pt/Au contacts on p-InGaAsP, and Au-Sn on n-InP are summarized in Table 2-4. In the measurement, mesas of thin conductive crystals on a semi-insulating InP substrate were used as thin conductive layer. The Cr/Pt/Au contact on p-InGaAsP crystal without Zn-diffusion showed non-ohmic characteristics. The differences between R_{SK} and R_{SH} are large for Au-Zn and Au-Sn, while R_{SK} is almost equal to R_{SH} for Cr/Pt/Au. These results correspond to the fact that Au-Zn and Au-Sn are alloy contacts, and Cr/Pt/Au is a non-alloy contact.

Table 2-4 Contact resistivity (ρ_c), sheet resistance beneath the contact (R_{SK}), and sheet resistance between the contact (R_{SH}) for Au-Zn and Cr/Pt/Au contacts on p-InGaAsP, and Au-Sn on n-InP.

CONTACT METAL	CRYSTAL (CARRIER CONC.)	ρ_c (Ωcm^2)	R_{SK} (Ω)	R_{SH} (Ω)
Au-Zn	p-InGaAsP (2×10^{18} cm^{-3})	9.2×10^{-5}	173	1163
Cr/Pt/Au	p-InGaAsP (Zn-DIFFUSED)	2.6×10^{-4}	70	92
Au-Sn	n-InP (1×10^{17} cm^{-3})	5.1×10^{-5}	48	200

2-7. Summary

In this chapter, the process technologies for the InGaAsP/InP materials system were described. The process conditions have been

examined for epitaxial growth, insulator film deposition, etching, dopant diffusion, and metallization. Especially for the etching and the metallization, new technologies, i.e., the reactive ion etching (RIE) with Br_2-containing gases and the transmission line model (TLM) method using a new contact arrangement have been proposed. The reliable technologies have been developed for all the processes, and they are applied to device fabrications described in the following chapters.

The important quantitative results obtained in this chapter are as follows:

1) The conditions of liquid-phase epitaxy (LPE) and organometallic vapor-phase epitaxy (OMVPE) have been determined for InP and InGaAs(P) as shown in Tables 2-2 and 2-3.
2) By using the RIE with a mixture of Br_2 and Ar gases, smooth vertical walls have been obtained for InGaAsP/InP crystals with a high etching rate of about 2 μm/min.
3) Based on a new TLM method, the contact resistivities of ohmic contacts on InGaAsP/InP have been evaluated as shown in Table 2-4.

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III. INTEGRATION OF A LASER DIODE AND A PASSIVE WAVEGUIDE
— INTEGRATED PASSIVE CAVITY (IPC) LASER —

3-1. Introduction

In this chapter, the integration of a laser diode and a passive waveguide is described. It performs signal generation in optical signal processings. Two new integrated structures, a self-aligned integrate loaded (SAIL) guide and a passive/active loaded (PAL) guide, are proposed. Three structures including these two and a bundle-integrated-guide (BIG) are fabricated. To achieve high efficiency in optical connection, the integrated structure should have a low guiding loss in the passive waveguide and a high coupling efficiency between the laser and the waveguide. The guiding loss and the coupling efficiency have been evaluated for the three integrated structures. Furthermore, the SAIL guide has been applied to the integrated passive cavity (IPC) laser consisting of an active cavity and a long passive cavity.

For the future optical signal processing systems, it is essential to have stable single frequency semiconductor lasers as optical sources. Although a number of device geometries have been proposed to achieve single longitudinal mode oscillation [1-5], further reductions of spectral linewidth and frequency chirping are required. On the other hand, long external cavity lasers constructed with an mirror or a diffraction grating have been proposed for the stabilization of oscillation frequency [6-9]. They have a short semiconductor gain medium with a long external cavity, where longer cavity is shown to be effective for the stabilization. To realize a mechanically stable device, however, it is desirable to use integrated configuration, that is, the IPC laser.

3-2. Integrated Device Structures

The structure of the SAIL guide is shown in Fig. 3-1 [10]. A loaded waveguide consisting of an n-InGaAsP ($\lambda_g = 1.1$ μm) waveguide layer and an n-InP load stripe is used as the passive cavi-

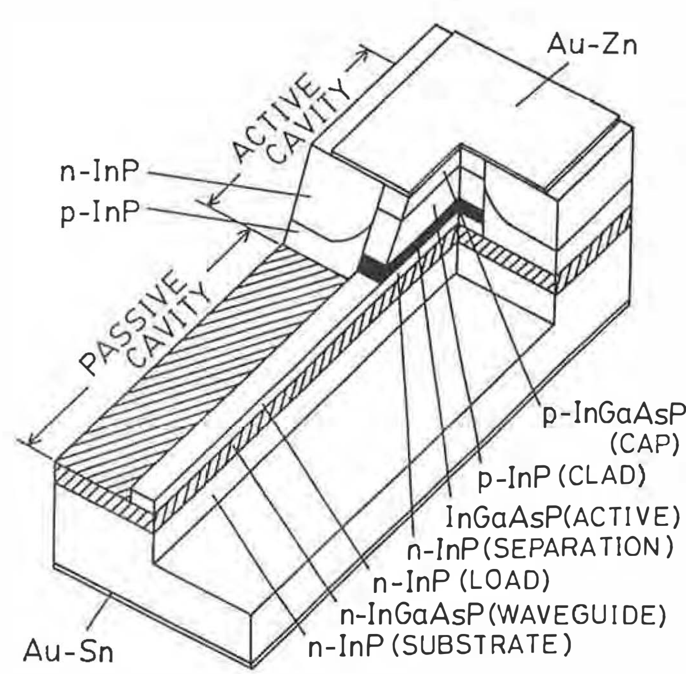

Fig. 3-1 Schematic view of the self-aligned integrated loaded (SAIL) guide structure.

ty, while the active cavity is a buried heterostructure (BH) laser. The loaded waveguide has lower guiding loss than ridge, rib, and BH waveguides. Furthermore, the load stripe of the passive cavity is self-aligned to the InGaAsP ($\lambda_g = 1.3\ \mu m$) active layer stripe, which was expected to reduce the optical coupling loss between the active and the passive cavities. However, the coupling efficiency of this structure is relatively low since the vertical mode of confined light is a first-order mode in the active cavity and a fundamental mode in the passive cavity. The fabrication steps of the SAIL guide structure is detailed in Section 3-3.

The schematic drawing of the PAL guide is shown in Fig. 3-2. In this structure, the loaded waveguide is adopted in the active cavity as well as the passive cavity. The active layer and the waveguide layer of the PAL guide are on the same plane to reduce the coupling loss between the active cavity and the passive cavity. In spite of this improvement, the coupling efficiency of the PAL guide is also relatively low since the thickness of the

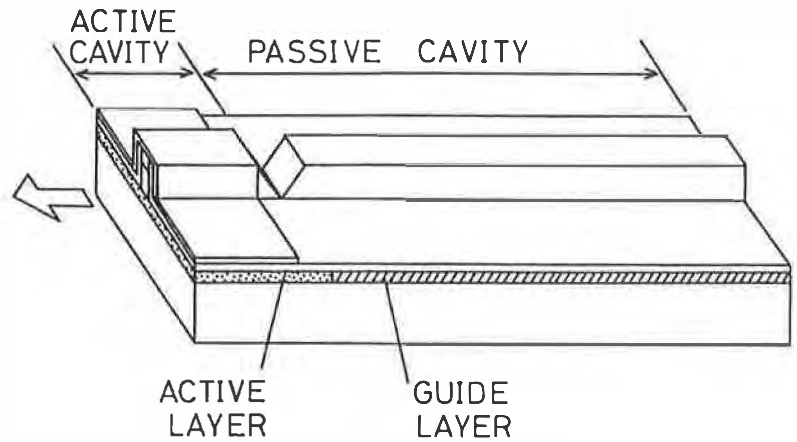

Fig. 3-2 Schematic view of the passive/active loaded (PAL) guide structure.

waveguide layer grown by the second LPE growth is not uniform and much larger than that of the active layer at the coupling point in the really fabricated device.

The third structure fabricated in this study is the BIG, which has high coupling efficiency between the active and the passive cavities not only theoretically but experimentally [11]. However, the guiding loss of the passive cavity is larger for the BIG-IPC laser compared with the SAIL guide and the PAL guide since it had a BH structure both in the active and the passive cavities as

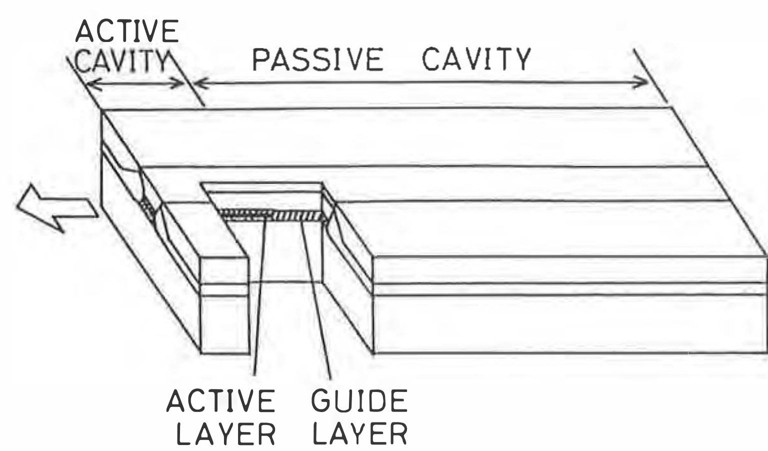

Fig. 3-3 Schematic view of the bundle-integrated-guide (BIG) structure.

shown in Fig. 3-3. The details of coupling efficiency and the guiding loss for these three structures are discussed in Section 3-5-1.

3-2. Fabrication

The fabrication steps of the SAIL guide structure are shown in Fig. 3-4. To fabricate it, six layers are first grown on a (100)-oriented n^+-InP substrate. They are an n-InP buffer layer ($\sim 5\ \mu m$, $3 \times 10^{18}\ cm^{-3}$), an n-InGaAsP waveguide layer ($0.5\ \mu m$, $5 \times 10^{17}\ cm^{-3}$, bandgap wavelength $\lambda_g = 1.05\ \mu m$), an n-InP separation layer ($0.1\ \mu m$, $1 \times 10^{18}\ cm^{-3}$), an InGaAsP active layer ($0.15\ \mu m$, undoped, $\lambda_g = 1.3\ \mu m$), a p-InP clad layer ($2\ \mu m$, $5 \times 10^{17}\ cm^{-3}$), and a p-InGaAsP cap layer ($0.5\ \mu m$, $2 \times 10^{18}\ cm^{-3}$, $\lambda_g = 1.1\ \mu m$). Then stripe mesa etching and regrowth of p-InP and n-InP are done as shown in Fig. 3-4(b)-(d). In mesa etching, the wafer is etched down to the surface of the waveguide layer using a SiO_2 stripe mask. The cap layer is etched by Br-CH_3OH. The clad layer, the active layer, and the separation layer are etched by preferential etchants:

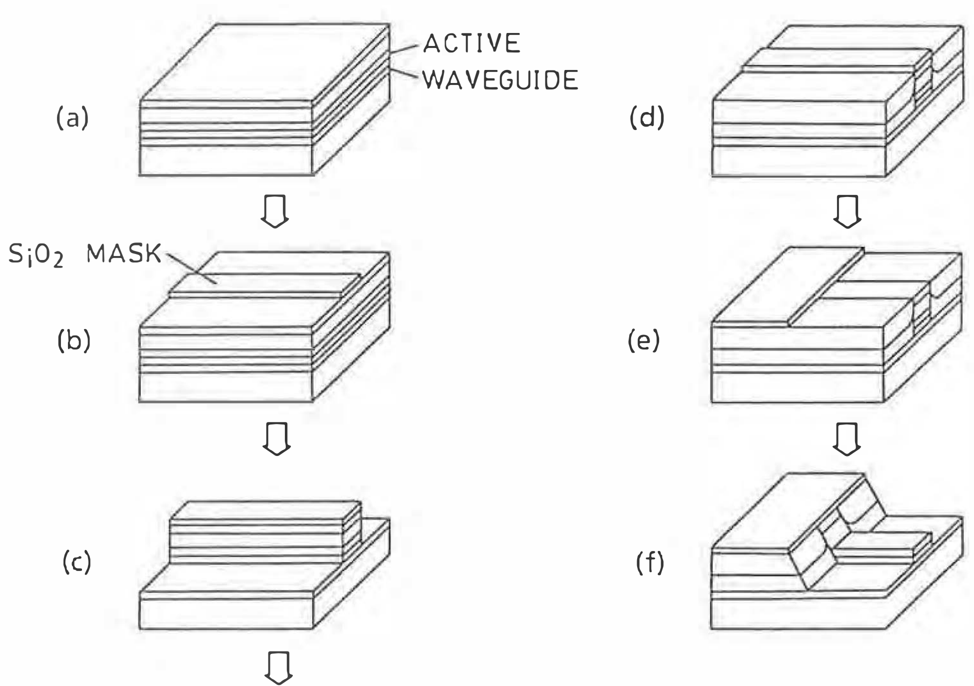

Fig. 3-4 Fabrication steps of the SAIL guide IPC laser.

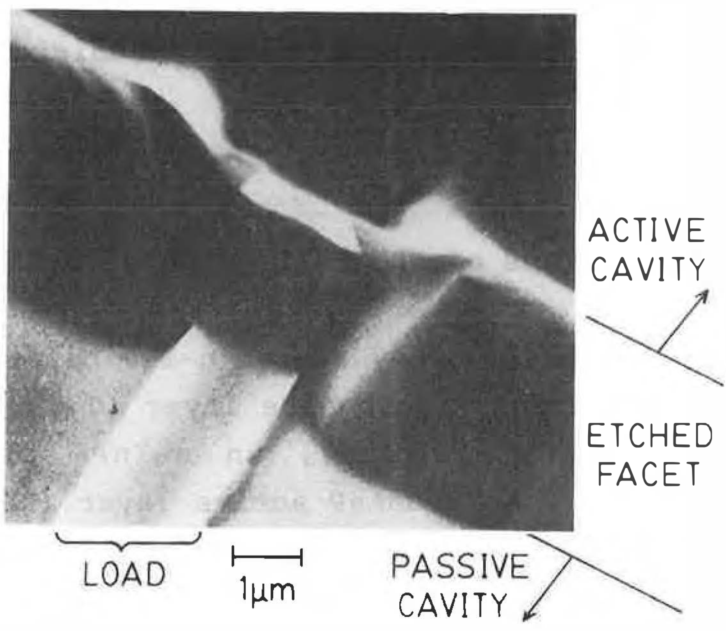

Fig. 3-5 SEM photograph of the SAIL guide at the coupling point of the active and the passive cavities.

$HCl:H_3PO_4$ (1:2 in volume) for InP and $H_2SO_4:H_2O_2:H_2O$ (1:1:5 in volume) for InGaAsP, to expose the surface of the waveguide layer. The stripe width of the active layer is about 2.0 μm.

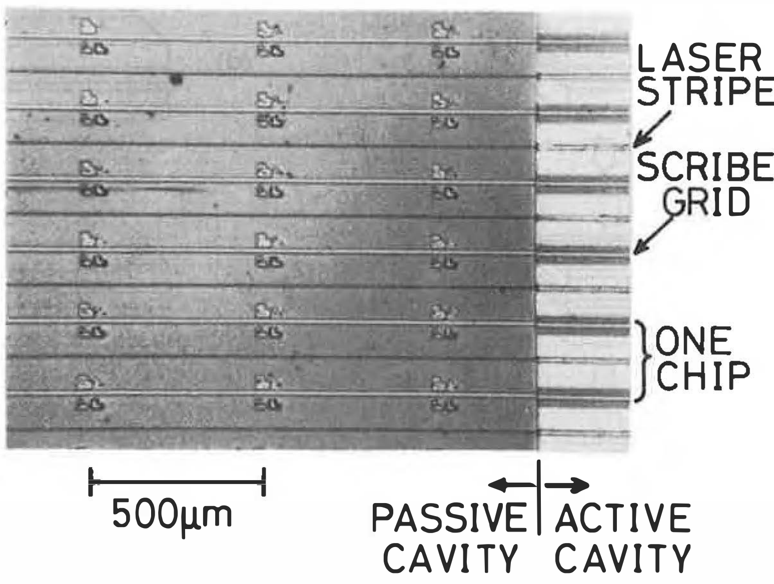

Fig. 3-6 Photomicrograph of the SAIL guide IPC lasers after wafer processes.

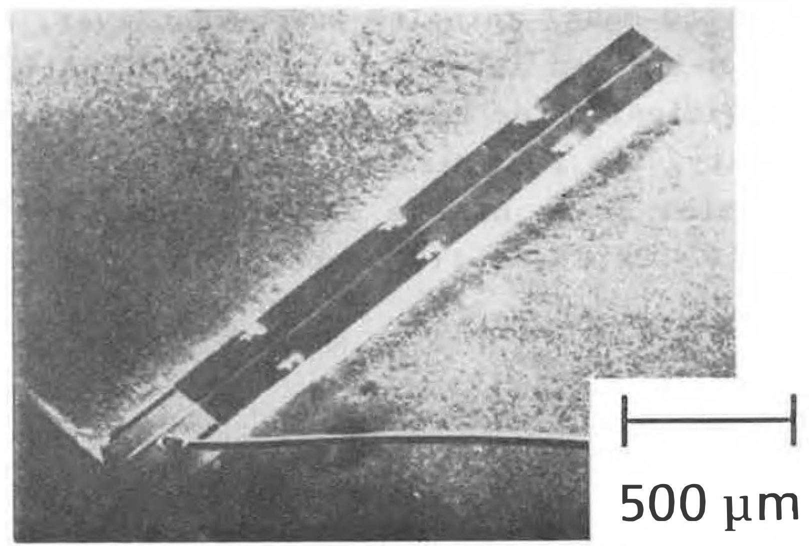

Fig. 3-7 SEM photograph of the SAIL guide IPC laser after assembly processes.

After the second growth, a part of the wafer, which will be the active cavity, is masked by SiO_2 as shown in Fig. 3-4(e). The unmasked region is etched by CCl_4 RIE to remove the cap layer and is then etched by the preferential etchants for InP. As a result, the waveguide layer is exposed, except for the stripe region where the active stripe is left as shown in Fig. 3-4(f). The active layer is easily etched off by H_2SO_4 solution, and then the separation layer is left in the stripe shape, which is the load self-aligned to the active stripe. The passive cavity is made of this load and the waveguide layer. The SEM photograph of the SAIL guide at the coupling point of the active and the passive cavities is shown in Fig. 3-5. After removing the SiO_2 mask, the Au-Zn contact is formed on the active cavity and the Au-Sn contact on the back of the substrate. The photomicrograph of the wafer after contact formation is shown in Fig. 3-6. The wafer is then cleaved and mounted on a package as shown in Fig. 3-7.

To fabricate a PAL guide IPC laser, the layers for the active cavity are first grown on an n^+-InP substrate. They are an n-InP buffer layer, an InGaAsP active layer, a p-InP clad layer, and a p-InGaAsP cap layer. Then a part of the wafer, which will be the

active cavity, is masked and the top three layers are etched off. After removing the mask, an n-InP waveguide layer, an n-InP clad layer, and an n-InP cap layer are grown both on the active and the passive cavities. After removing the secondly grown layers on the active cavity, the load stripe is formed.

The fabrication steps of the BIG-IPC laser are the same as those of the BIG-DBR laser [11] except that DBR corrugation is not formed.

3-4. Characteristics

3-4-1. Threshold current

The current - output power characteristics of SAIL guide IPC lasers at room temperature pulse operation are shown in Fig. 3-8, where (a) is a long IPC laser, (b) a short IPC laser, and (c) a conventional laser. The passive/active cavity length ratios (denoted by L_{PC}/L_{AC}) of the long and short IPC lasers are 3553 μm/400 μm (= 8.88) and 273 μm/224 μm (= 1.22), and the conventional laser has a 248 μm-long cavity, which is the same geometry as the active cavity of the SAIL guide IPC lasers. As shown in Fig. 3-8, the long IPC laser has a lower threshold current of 58 mA than the short IPC laser with a threshold of 72 mA, though the conventional laser has the lowest threshold of 31 mA.

To clear the relation between the threshold current and the length of the passive cavity, threshold currents have been measured for IPC lasers with different passive cavity lengths. The results are shown in Fig. 3-9, where no relation is observed between them. Two reasons can be considered for this. One is that the main reflection of the passive cavity side occurs at the coupling point of the active and the passive cavities. In this case, the coupling efficiency and the guiding loss related to the passive cavity length do not affect the threshold current. The other is that increasing of the threshold current is not due to the guiding loss but to the coupling loss though the main reflection occurs at the end facet of the passive cavity.

The experiment described below was carried out to distinguish the main reflecting point. The characteristics of the laser with

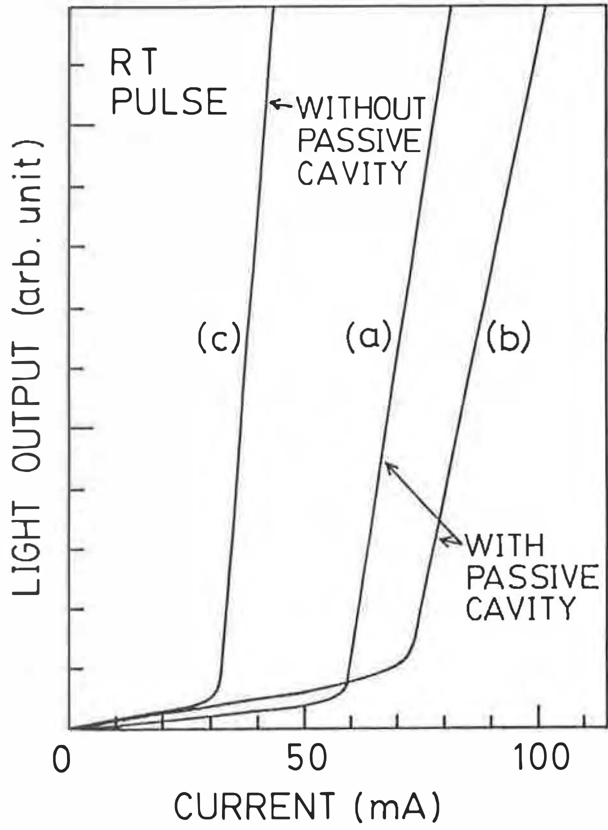

Fig. 3-8 Current - output power characteristics: (a) a long IPC laser, (b) a short IPC laser, and (c) a conventional laser having the same structure as the active cavity of the IPC laser. The passive/active cavity length ratios of the long and short IPC lasers are 3553 μm/400 μm and 273 μm/224 μm, and the conventional laser has a 248 μm-long cavity.

a structure shown in Fig. 3-10 was first measured. In this structure, an additional active cavity suppressed the reflection from the end facet of the passive cavity. Then the laser was cleaved to remove the additional active cavity and the characteristics were measured again. The laser with an additional active cavity did not oscillate up to a driving current of 200 mA, while the laser without it had a threshold current of 150 mA. The threshold current was further reduced to 86 mA by evaporating Au on the end facet of the passive cavity as a reflection coating. These results shows that the reflection at the end facet of the passive cavity is important for laser oscillation. Therefore, the reason

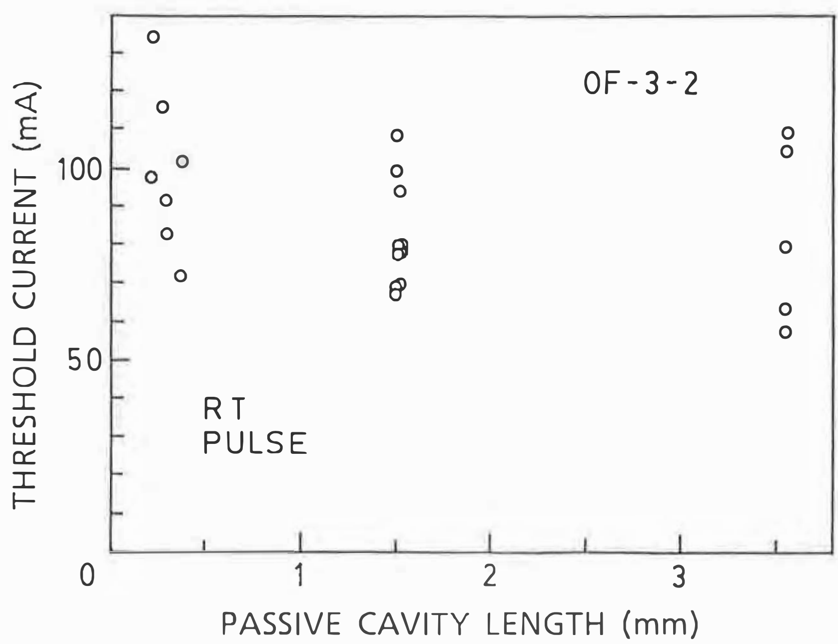

Fig. 3-9 Relation between the threshold current and the passive cavity length for SAIL guide IPC lasers.

why threshold current of the SAIL guide IPC lasers does not depend on the passive cavity length is attributed that the coupling efficiency is the dominant factor which increases the threshold

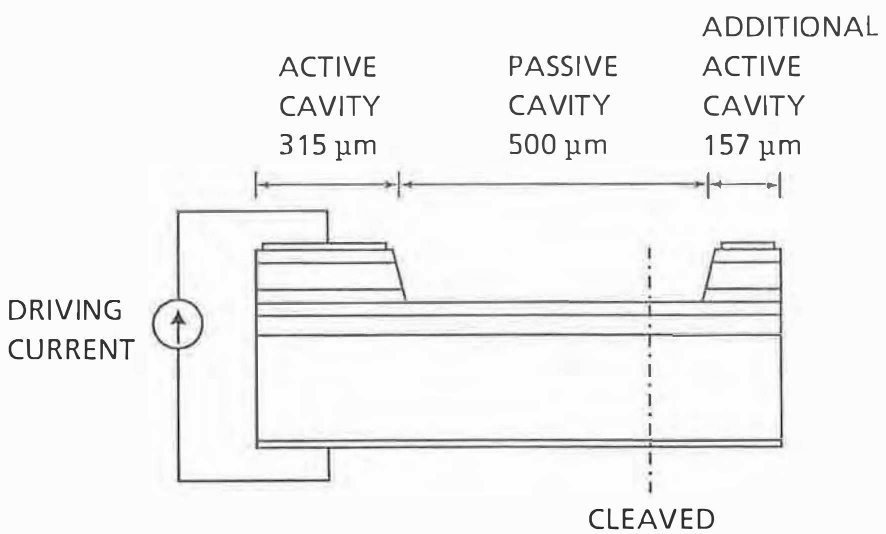

Fig. 3-10 Structure of the test sample to clear the reflecting point on the passive cavity side for the SAIL guide.

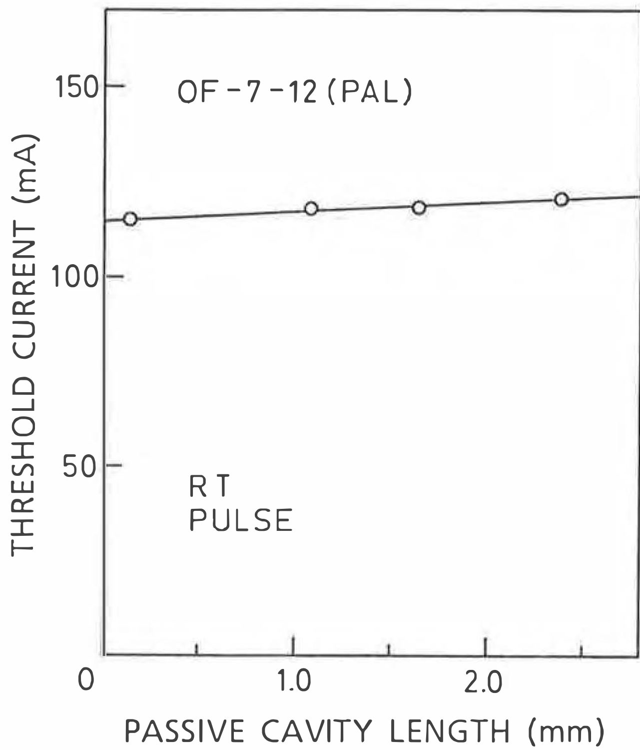

Fig. 3-11 Relation between the threshold current and the passive cavity length for a PAL guide IPC laser. In this measurement, the same laser was cleaved to be shorter to vary the cavity length.

current.

The relation between the threshold current and the passive cavity length has also been measured for the PAL-IPC and the BIG-IPC lasers. The results are shown in Figs. 3-11 and 3-12. For these lasers, a laser with a longer passive cavity has a larger threshold current since the measurement was done by cleaving the same lasers. The threshold current of the PAL-IPC laser does not strongly depend on the passive cavity length. On the other hand, the threshold current of BIG-IPC laser is affected by the passive cavity length and the laser with a passive cavity longer than 1 mm does not oscillate at all. These results proves that the guiding loss of a BH waveguide is much larger than that of a loaded waveguide.

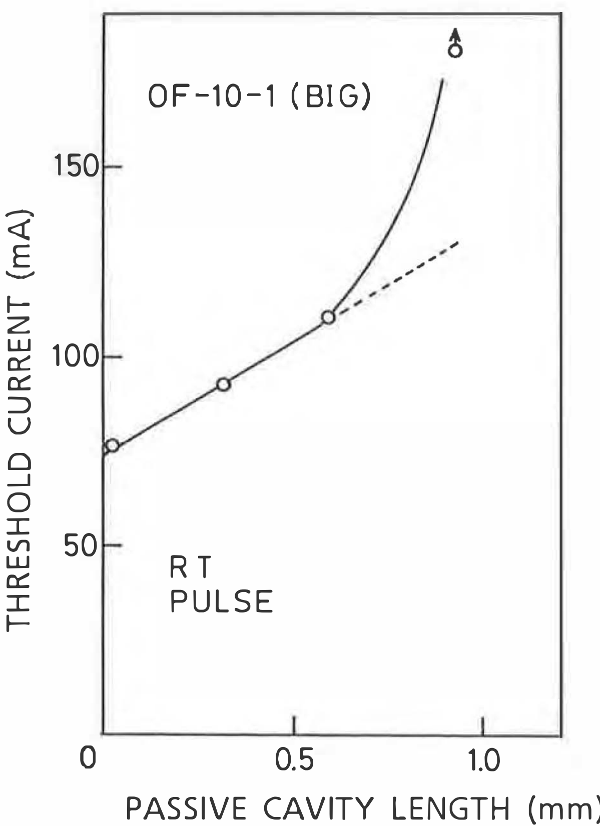

Fig. 3-12 Relation between the threshold current and the passive cavity length for a BIG-IPC laser. In this measurement, the same laser was cleaved to be shorter to vary the cavity length.

3-4-2. Longitudinal mode

The SAIL guide IPC laser exhibited stable single longitudinal mode oscillations just above the threshold, whereas the laser without passive cavity showed the multimode oscillation. The longitudinal mode characteristics of the long IPC laser, measured at 20 °C, CW operation for several driving current, are shown in Fig. 3-13. By increasing the driving current, the oscillation mode is transferred to a shorter wavelength mode with a mode spacing of about 18 Å. This mode transfer is due to the mode selectivity of the coupled cavity and is well explained by the phase and gain conditions as described in Section 3-5-2.

From the viewpoint of mode selectivity in a coupled cavity laser, it is considered that $L_{PC}/L_{AC} < 1$ is favorable for stable

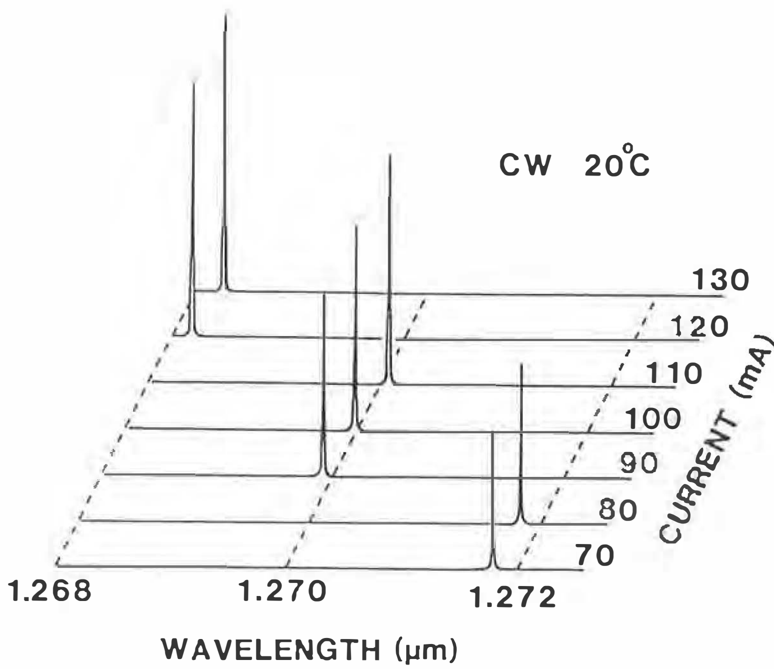

Fig. 3-13 Longitudinal mode characteristics of the 3.55 mm-long IPC laser measured at 20 °C, CW operation for several driving currents.

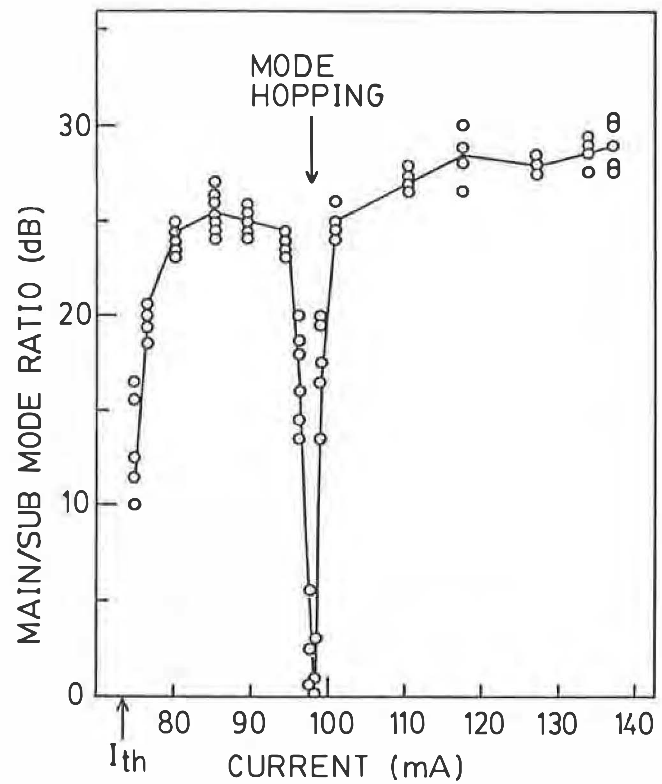

Fig. 3-14 Ratio of main longitudinal mode to submode in relation to the driving current.

single longitudinal mode operation [5]. The long IPC laser ($L_{PC}/L_{AC} = 8.9$), however, showed a clean single mode oscillation. The ratio of main longitudinal mode to submode is shown in Fig. 3-14. The maximum side-mode suppression ratio exceeds 30 dB.

3-4-3. Spectral linewidth

The spectral linewidth of the IPC laser was measured by utilizing a delayed self-heterodyne technique [12]. An acousto-optic modulator was used to obtain a 120 MHz frequency shift, and a conventional single-mode fiber (length 5 km) was used as the optical delay line. The resolution of this system is 40 kHz. Assuming a Lorentzian lineshape, the linewidth of full-width at half-maximum (FWHM) is obtained as half the measured FWHM of the beat spectrum recorded on a spectrum analyzer [13,14]. Great care was taken to eliminate reflection from various optical components by using two optical isolators.

An IPC laser with the active and passive cavity lengths of 265 μm and 1518 μm was used for the measurement of spectral linewidth. The end facet of the passive cavity was coated with Au to increase the reflectivity, which is effective not only for reduc-

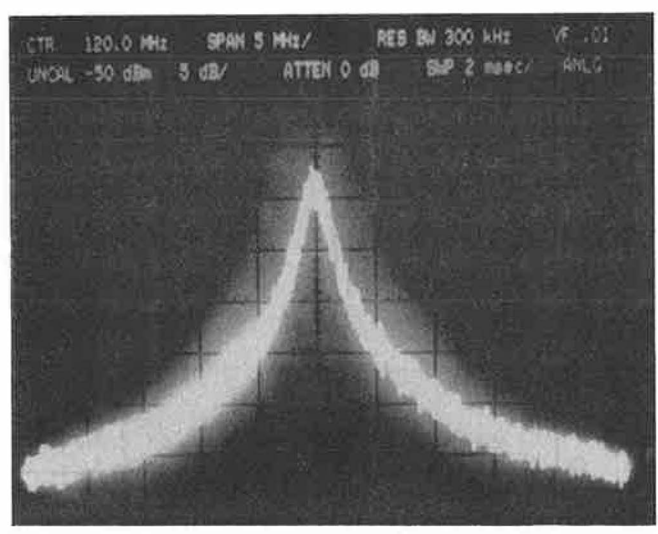

Fig. 3-15 Beat spectrum corresponding to the spectral linewidth of 900 kHz measured for an IPC laser with a passive cavity length of 1.51 mm.

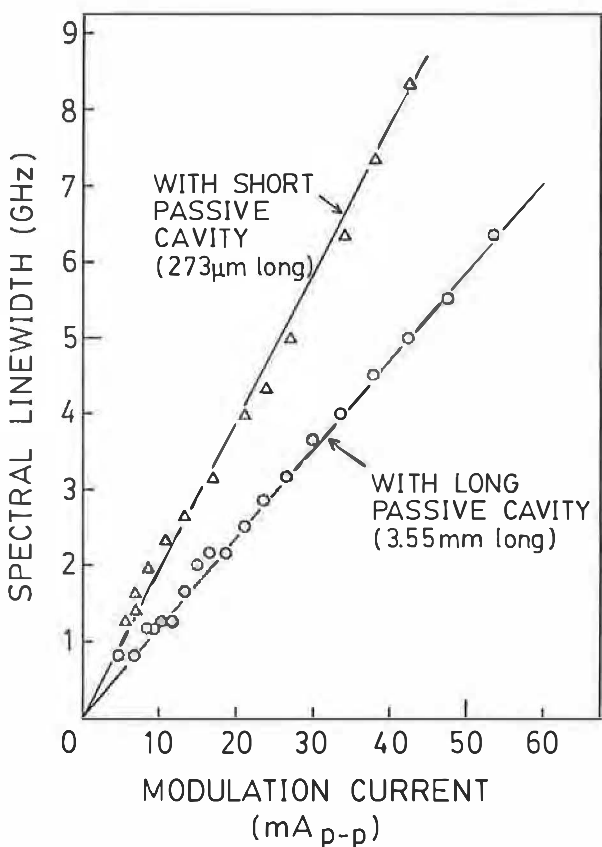

Fig. 3-16 Spectral linewidths under amplitude modulation for the IPC lasers with passive cavity lengths of 273 μm and 3.55 mm.

ing threshold current but also for narrowing linewidth [9,15]. The linewidth is changed by the driving current and the temperature of the laser in association with the longitudinal mode spectra. The linewidth is narrowed when the longitudinal submode is suppressed, while it is broadened when the submode appeared. However, the linewidths of 1 - 2 MHz are easily obtained and the minimum value is about 900 kHz which was achieved at 8 °C CW operation with a driving current of 128 mA and an output power of 6 mW. The measured beat spectrum of about 900 kHz is shown in Fig. 3-15.

In addition to the linewidth narrowing, the IPC laser has another advantage in the reduction of frequency chirping. The spectral linewidths under amplitude modulation are shown in Fig. 3-16. The long IPC laser has narrower linewidths than the

short IPC laser, which indicates the longer passive cavity is more effective for the reduction of frequency chirping.

3-5. Discussion

3-5-1. Coupling efficiency and guiding loss

Threshold current density (J_{th}) of an injection laser is given by [16]

$$J_{th} = J_0 d/\eta + d/\eta\Gamma\beta[\alpha_i + (1/2L_{AC})\ln(1/R_1R_2)] \quad (3\text{-}1)$$

(d: active layer thickness, L_{AC}: active cavity length, R_1 and R_2: reflectivities of the both facets, β and J_0: slope and offset in the relation between gain and nominal current, η: internal quantum efficiency, Γ: confinement factor, and α_i: guiding loss of the active cavity). Therefore, threshold current (I_{th}) is expressed as

$$I_{th} = k\,[\alpha_{eff}L_{AC} + (1/2)\ln(1/R_1R_2)], \quad (3\text{-}2)$$

where $k = dW/\eta\Gamma\beta$ (W: active stripe width) (3-3)

and $\alpha_{eff} = \Gamma\beta J_0 + \alpha_i$. (3-4)

In case of the IPC laser, assuming that the main reflecting point is the end facet of the passive cavity, the reflectivity of passive cavity side (R_2) is given by

$$R_2 = R_1\,\eta_c^2 \exp(-2\,\alpha_{PC}\,L_{PC}), \quad (3\text{-}5)$$

where R_1 is the reflectivity of cleaved facet, η_c is the coupling efficiency, α_{PC} is the guiding loss of passive cavity, and L_{PC} is the passive cavity length. Combining Eqs. (3-2) and (3-5), the following equation is obtained.

$$I_{th} = k\,[\alpha_{eff}L_{AC} + \ln(1/R_1) + \alpha_{PC}L_{PC} + \ln(1/\eta_c)] \quad (3\text{-}6)$$

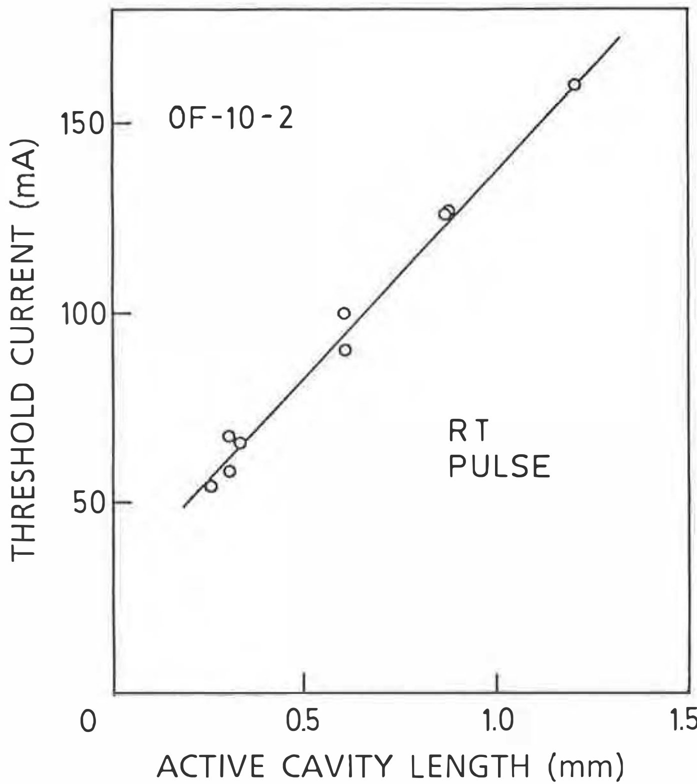

Fig. 3-17 Relation between the threshold current and the active cavity length for the BIG-IPC lasers without passive cavities.

By using Eq. (3-6), α_{PC} and η_{PC} can be estimated as follows. First, the relation between threshold current and active cavity length is measured for the laser without the passive cavity, which gives the values of k and α_{eff}. An example of the relation for the BIG-IPC lasers is shown in Fig. 3-17. In this case, k and α_{eff} are 25.0 mA and 43.4 cm^{-1}, respectively. Then the relation between the threshold current and passive cavity length is measured as shown in Figs. 3-11 and 3-12, which gives the values of α_{PC} and η_{C}. The values obtained for three types of IPC lasers are summarized in Table 3-1.

As seen from Table 3-1, the SAIL guide and the PAL guide have low coupling efficiency and low guiding loss, while the BIG has high coupling efficiency and high guiding loss. To obtain both high coupling efficiency and low guiding loss, combination of the

Table 3-1 Coupling efficiency and guiding loss of three types of IPC lasers.

STRUCTURE	COUPLING EFFICIENCY η_C (%)	GUIDING LOSS α_{PC} (cm^{-3})
SAIL GUIDE	< 36	~ 1
PAL GUIDE	< 29	1.2
BIG	> 67	24.0

PAL and the BIG is thought to be the best, that is, the layer structures of the active and passive cavities are just the same as the BIG and both cavities have a loaded waveguide structure [17]. Though the PAL-BIG-IPC laser has not been fabricated yet, it is expected to have low threshold current and good characteristics in frequency stabilization. Furthermore, the PAL-BIG structure can easily be applied to other photonic IC's since it has an advantage in productivity owing to simple fabrication steps.

3-5-2. Analysis for longitudinal mode

The mode transfer observed for the long IPC laser described in Section 3-4-2 has been analyzed by using the phase and gain conditions of the coupled cavity. Device parameters of a model of the IPC lasers are denoted in Fig. 3-18(a), where r_1, r_2, and r_3 are the amplitude reflectivities of each boundary, and n_1 and n_2 are the refractive indices of the active and the passive cavities, respectively. The phase conditions of this laser is written in the form [8,9,18]

$$\tan \phi_1 = f(\phi_2) \tag{3-7}$$

with

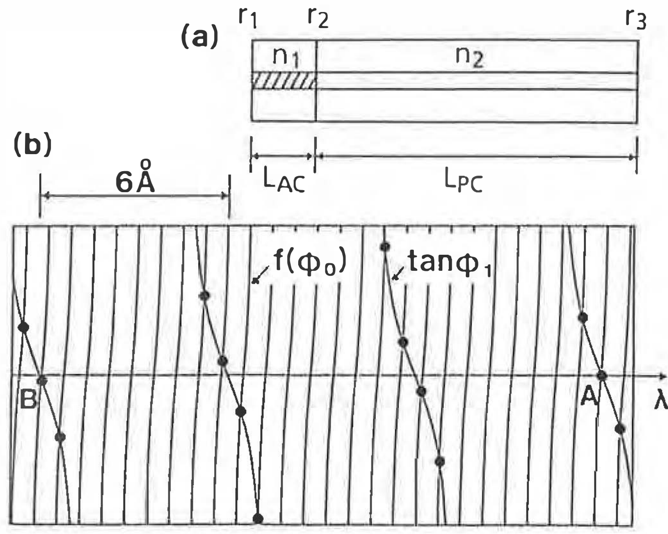

Fig. 3-18 Phase condition for the 3.55 mm-long IPC laser in relation to the oscillation wavelength λ.

$$f(\phi_2) = r_3(r_2^2-1)\sin\phi_2/[r_2(1+r_3^2)+r_3(1+r_2^2)\cos\phi_2]. \quad (3\text{-}8)$$

Here, $\phi_1 = 4\pi n_1 L_{AC}/\lambda$ and $\phi_2 = 4\pi n_2 L_{PC}/\lambda$, and λ is the oscillation wavelength in vacuum.

The relations of λ vs $\tan\phi_1$ and $f(\phi_2)$ are shown in Fig. 3-18(b) with $L_{AC} = 400\ \mu m$, $L_{PC} = 3553\ \mu m$; $n_1 = 3.41$, $n_2 = 3.215$; $r_2 = 0.1$, $r_3 = 0.2$. Each cross point of both curves gives the wavelength of a longitudinal mode. As L_{PC} is much larger than L_{AC} in this laser, there exist many modes that can be excited in the neighborhood of an active cavity mode. In this figure, however, only mode A is excited, because it has the least threshold gain [8]. Since the modes next to mode A have larger threshold gain and the mode with the second least threshold gain (denoted as mode B) exists with a spacing of about 18 Å, the longitudinal mode of the laser is transferred with this spacing.

3-6. Summary

In this chapter, the integration of a laser diode and a passive waveguide was described. It is the integration in optical

signal generation. Two new integrated structures, i.e., a self-aligned integrate loaded (SAIL) guide and a passive/active loaded (PAL) guide have been proposed. Three structures including these two and a bundle-integrated-guide (BIG) have been fabricated. The integrated devices have been evaluated as an integrated passive cavity (IPC) laser consisting of an active cavity and a long passive cavity.

In regard to the coupling efficiency between the active and the passive cavities (η_C) and the guiding loss in the passive cavity (α_{PC}), the SAIL and the PAL have low η_C and low α_{PC}, while the BIG has high η_C and high α_{PC}. To obtain both high η_C and low α_{PC}, combination of the PAL and the BIG is thought to be the best. The SAIL guide IPC laser exhibits stable single longitudinal mode oscillation and shows favorable effects for the frequency stabilization, such as the narrowing of spectral linewidth and the reduction of frequency chirping.

The important quantitative results obtained in this chapter are as follows:

1) A SAIL guide IPC laser with a 3.55 mm-long passive cavity has successfully been fabricated and operated with a rather low threshold current of 58 mA.
2) The threshold currents of the SAIL, the PAL, and the BIG-IPC lasers have been measured in relation to the passive cavity length, from which η_C and α_{PC} are evaluated as shown in Table 3-1.
3) The long IPC laser exhibits stable single longitudinal mode oscillation with the maximum side-mode suppression ratio of more than 30 dB.
4) The mode of the long IPC laser transfers with a mode spacing of 18 Å, which coincides with the result of theoretical analysis by using the phase and gain conditions.
5) The spectral linewidth of the IPC laser has been measured by utilizing a delayed self-heterodyne technique. The linewidths of 1 - 2 MHz are easily obtained and the minimum value is about 900 kHz at the output power of 6 mW.

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IV. INTEGRATION OF A PIN PHOTODIODE AND AN AMPLIFIER CIRCUIT — MONOLITHIC PHOTORECEIVER —

4-1. Introduction

In this chapter, a monolithic photoreceiver incorporating a photodiode and a preamplifier is described. It is the integration in optical signal detection, and is a typical OEIC incorporating an optoelectronic device and an electronic circuit. The monolithic photoreceiver is very attractive for high speed and low noise operation since the integration can reduce the front-end capacitance [1-7]. Recent progress of GaAs-based monolithic photoreceivers are noticeable [5-7] and a very wide bandwidth of 5.2 GHz has been achieved [7]. GaAs-based optoelectronic devices, however, cannot be applied to long wavelength optical communication systems. InP-based devices are necessary to be integrated for that application though InP-based electronic devices are not so matured as GaAs-based ones.

In this study, a monolithic photoreceiver based on the InGaAs/InP materials system has been developed [8,9]. The fabricated photoreceiver consists of an InGaAs pin photodiode (PD) and a transimpedance preamplifier in which four junction field effect transistors (FET's), four level shift diodes, and a feedback resistor are integrated. The whole circuit is designed to operate with a single 5V power supply. The 5V operation of photoreceiver is a key to simplify the whole transmission system since most logic IC's are operated with a 5V power supply. In addition, easily producible device structures have been adopted to increase the yield of the photoreceivers. The simplicity in fabrication and the usability in application are considered to be essential to make OEIC's practical.

4-2. Integrated Circuit Design

4-2-1. Device structures

The structure of the pin PD and the junction FET integrated in the photoreceiver are shown in Fig. 4-1. The PD is constructed with an n^--InGaAs layer having a Zn diffused p-type region and an

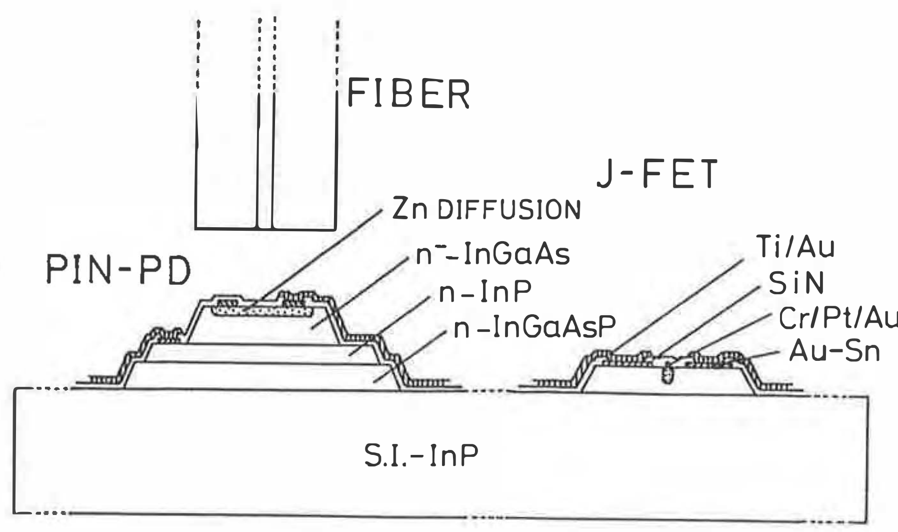


Fig. 4-1 Schematic cross-section of the pin PD and the junction FET integrated in the monolithic photoreceiver.

n-InP layer to reduce the series resistance of the PD. The diameter of the photosensitive area is designed to be 80 μm to permit optical coupling with a multimode optical fiber. The Zn-diffused region has a diameter of 100 μm including an area for a ring anode and a margin between the anode and the edge of the diffused area. The FET is fabricated by using an n-InGaAsP (bandgap wavelength λ_g =1.1 μm) layer with a gate diffusion. The gate length was first designed to be 6 μm for easiness of fabrication. A gate length of 3 μm is adopted later to improve the frequency characteristics.

Not shown in Fig. 4-1, a level shift diode has the same p-n junction as the gate-source of the FET, and a feedback resistor is made of the n-InGaAsP layer without diffusion. The level shift diodes are used to give DC bias voltage for the FET's. The value of the feedback resistor is designed to be 1.2 kΩ or 3.6 kΩ. The latter value is adopted in high-sensitive photoreceivers though it degrades the bandwidth.

To operate the whole circuit with a single 5 V power supply, the FET should have low saturation voltage which means that shallow channel depth is desirable. However, a shallow channel decreases the transconductance. Therefore, precise control of chan-

nel depth is important to make 5 V operation consistent with high speed operation. As seen in Fig. 4-1, the channel depth is the difference between the InGaAsP layer thickness and the gate diffusion depth. Since the InGaAsP layer is grown by LPE and it is difficult to control the layer thickness exactly by LPE, the diffusion depth was adjusted for the monitored layer thickness. The quantitative design for channel depth is described in the following section.

4-2-2. DC bias point

The circuit of the photoreceiver is shown in Fig. 4-2. The DC bias point of the circuit has been considered as follows to optimize the channel depth of the FET's. Since drain current (I_{Di}) of FET Q_i ($i = 1 - 4$) is a function of drain-source voltage (V_{Di}) and gate-source voltage (V_{Gi}), following equations are obtained for the amplifier stage:

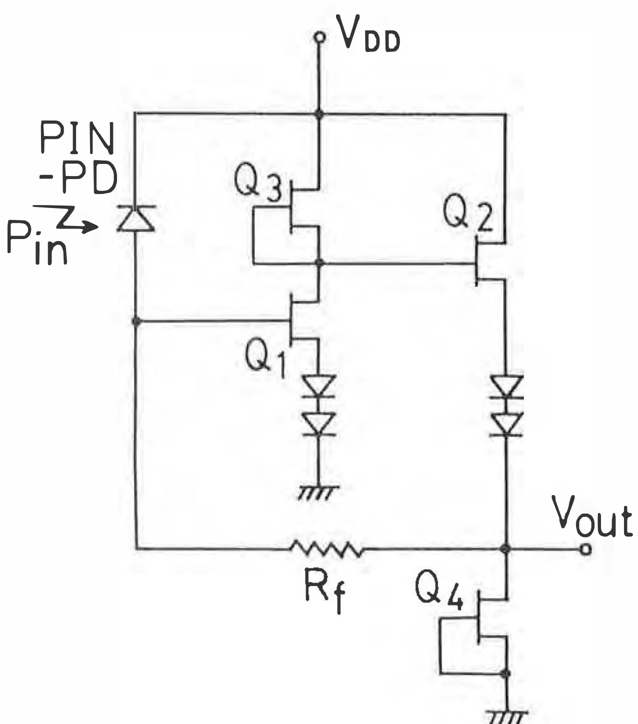


Fig. 4-2 Circuit diagram of the monolithic photoreceiver consisting of a pin photodiode (PD) and a transimpedance preamplifier.

$$I_{D1} = f_1(V_{D1}, V_{G1})$$

$$= f_1(V_{D1}, V_{D1} - V_{G2} - V_{LS} + R_f I_p) \quad (4\text{-}1)$$

$$I_{D3} = f_3(V_{D3}, 0)$$

$$= f_3(V_{DD} - V_{D1} - V_{LS}, 0) \quad (4\text{-}2)$$

where V_{DD} and V_{LS} are the power supply voltage and the voltage shift of two level shift diodes, and R_f and I_p are the feedback resistance and the current of the PD. Eqs. (4-1) and (4-2) can be solved graphically for V_{D1} and I_{D1} ($= I_{D3}$) as illustrated in Fig. 4-3(a). In the figure, V_{DD}, V_{LS}, and I_p are set to be 5 V, 1.6 V, and 0, respectively, and V_{G2} is an unknown parameter.

On the other hand, following equations are obtained for the buffer stage:

$$I_{D2} = f_2(V_{D2}, V_{G2})$$

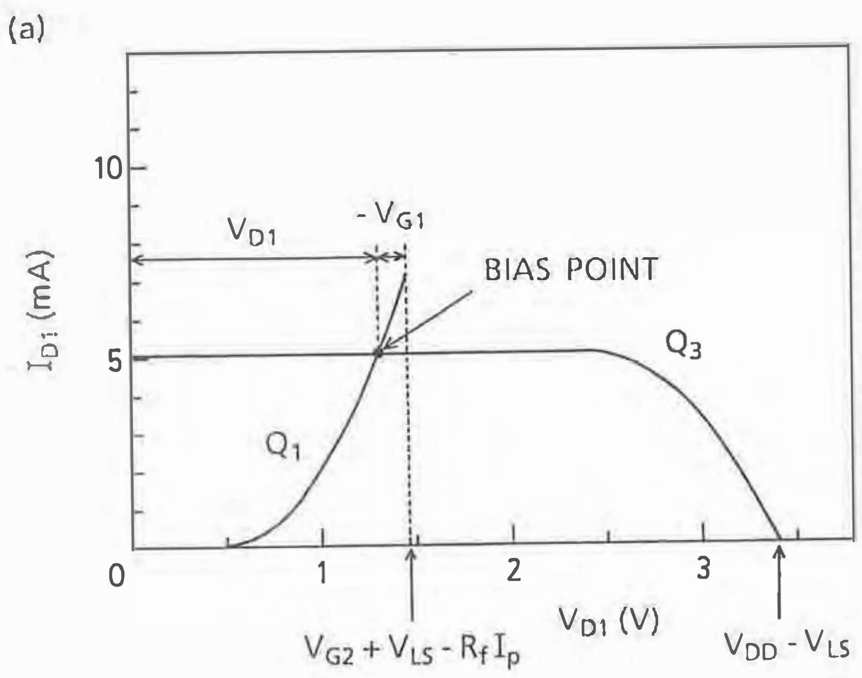
$$= f_2(V_{D2}, V_{D2} - V_{DD} + V_{D1} + V_{LS}) \quad (4\text{-}3)$$

$$I_{D4} = f_4(V_{D4}, 0)$$

$$= f_4(V_{DD} - V_{D2} - V_{LS}, 0). \quad (4\text{-}4)$$

Eqs. (4-3) and (4-4) can also be solved graphically for V_{D2} and I_{D2} ($= I_{D4}$) as illustrated in Fig. 4-3(b) though V_{D1} is an unknown parameter in it. Since the unknown parameter in Fig. 4-3(b) (V_{D1}) is obtained from Fig. 4-3(a) and the unknown parameter in Fig. 4-3(a) (V_{G2}) is obtained from Fig. 4-3(b), self-consistent solutions for Eqs.(4-1)-(4-4) give all the voltages in the circuit. In case that all FET's operate in saturation region, the solutions can easily be obtained since V_{G2} is determined only by using Fig. 4-3(b).

The function f_i is theoretically given by [10]



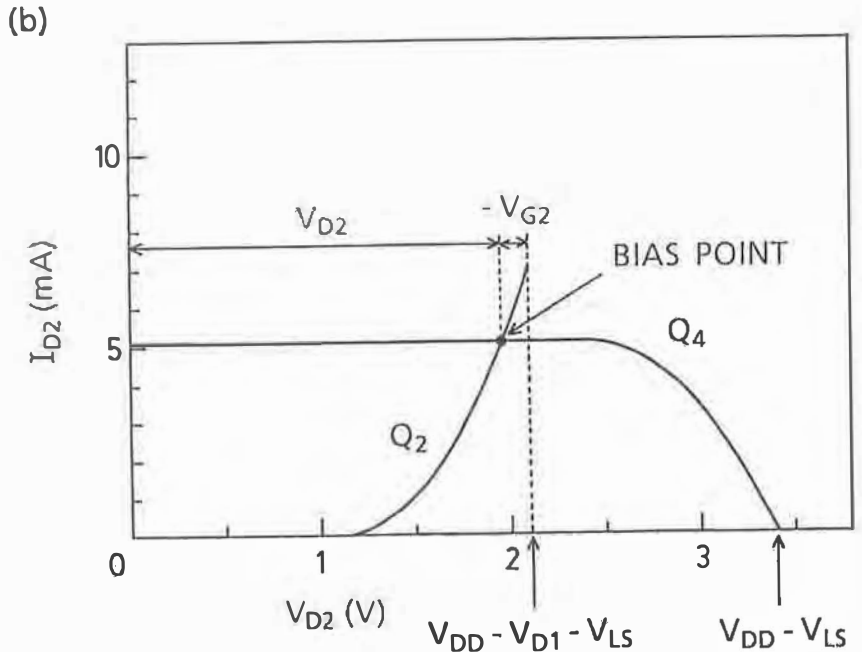


Fig. 4-3 Voltage - current characteristics for either (a) amplifier stage or (b) buffer stage to obtain the graphical solution of DC bias points.

$$I_D = 2W\mu qN_Dd/L\{V_D-(2/3d)(2\varepsilon_s/qN_D)^{1/2}[(V_D+V_{bi}-V_G)^{3/2} -(V_{bi}-V_G)^{3/2}]\} \quad \text{(in linear region)} \quad (4\text{-}5)$$

$$I_D = 2W\mu q^2N_D{}^2d^3/6\varepsilon_sL\{1-3[(V_{bi}-V_G)/V_p)]+2[(V_{bi}-V_G)/V_p]^{3/2}\} \quad \text{(in saturation region)} \quad (4\text{-}6)$$

where

$$V_p = QN_Dd^2 / 2\varepsilon_s \quad (4\text{-}7)$$

$$V_{bi} = kT/q \ln(N_AN_D/n_i{}^2). \quad (4\text{-}8)$$

The names and values of symbols in Eqs. (4-5)-(4-8) are summarized in Table 4-1. The curves in Fig. 4-3 are numerically calculated using these equations for the channel depth of 0.5 μm. In this case, all FET's operates in saturation region. Assuming d is 0.6 μm, however, the bias points of FET's Q_1 and Q_4 move to linear region, which is thought to reduce the output response for input photocurrent.

Table 4-1 Names and values of the symbols used in Eqs. (4-5) - (4-8).

SYMBOL	NAME	VALUE
μ	ELECTRON MOBILITY	3500 $cm^2/V\,s$
ε_s	DIELECTRIC CONSTANT	12.4 ε_0
n_i	INTRINSIC CARRIER DENSITY	3×10^{10} cm^{-3}
N_A	ACCEPTOR DENSITY IN GATE	5×10^{18} cm^{-3}
N_D	DONOR DENSITY IN CHANNEL	1×10^{16} cm^{-3}
L	GATE LENGTH	6 μm
W	GATE WIDTH (Q_1, Q_2)	500 μm
	(Q_3, Q_4)	350 μm
d	CHANNEL DEPTH	0.5 μm

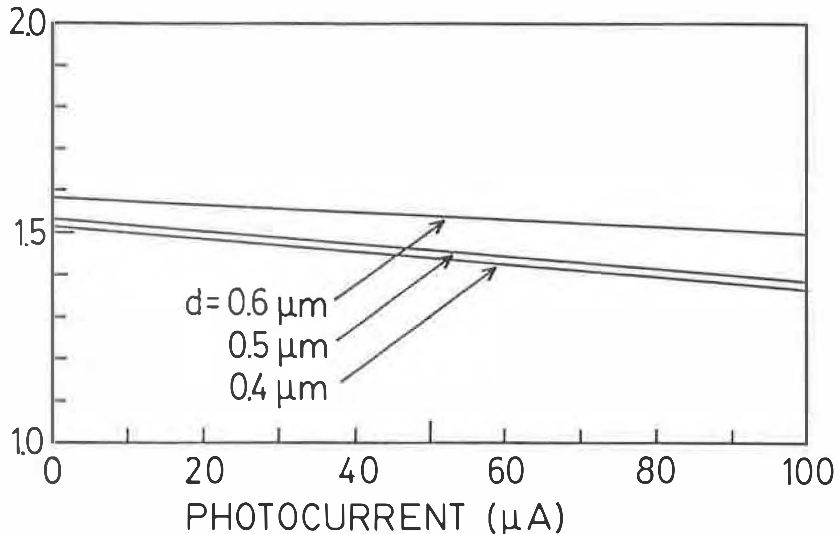


Fig. 4-4 Relation between input photocurrent and output voltage obtained by computer circuit simulation. The device parameters were determined based on Eqs. (4-5) - (4-8) with values shown in Table 4-1.

To confirm this effect, the relations between the input photocurrent and the output voltage have been simulated with a computer circuit simulator for d = 0.4, 0.5, and 0.6 µm. The results are shown in Fig. 4-4. The transimpedance, which is the ratio of output voltage change to input photocurrent, for d = 0.4 or 0.5 µm is approximately the same as the value of feedback resistance (1.5 kΩ), while that for d = 0.6 µm is smaller than this value. Therefore, the channel depth should be less than 0.5 µm for normal circuit operation. On the other hand, as the channel depth is decreased, transconductance and cutoff frequency of FET are decreased which degrades the frequency response as described in the following section. Considering these two factors, the optimum value of the channel depth is 0.5 µm.

4-2-3. Frequency response

The frequency dependence of the transimpedance (Z_t) is given by

$$Z_t(f) = -A R_f \,/\, (1 + A + if \,/\, f_{ci}), \qquad (4\text{-}9)$$

where R_f is the feedback resistance, A is the open loop gain of the amplifier, and f_{ci} is the cutoff frequency determined by R_f and a front-end capacitance (C_i), that is, $(2\pi C_i R_f)^{-1}$. The frequency dependence of A is given by

$$A(f) = A_0 \,/\, (1 + if \,/\, f_{ca}), \qquad (4\text{-}10)$$

where A_0 is the low frequency gain and f_{ca} is the cutoff frequency of the amplifier. As for the circuit shown in Fig. 4-2, A_0 is given by $g_{m1}(r_{ds1}//r_{ds3})$ where g_{m1} is a transconductance of the FET Q_1, and r_{ds1} and r_{ds3} are output resistance of the FET's Q_1 and Q_3, respectively.

$Z_t(f)$ can be calculated by combining Eqs. (4-9) and (4-10), but it does not give a simple solution for 3 dB bandwidth (f_{3dB}) of the photoreceiver. To clear the factors which limit f_{3dB}, two extreme cases are considered. In case of $f_{3dB} << f_{ca}$, A can set to be A_0 in Eq.(4-9) and f_{3dB} is given by

$$f_{3dB} = (1 + A_0)\, f_{ci}. \qquad (4\text{-}11)$$

This simple equation can be applied to most photoreceivers and is often treated as general expression [7,11,12]. In this case f_{3dB} is limited by f_{ci} and A_0. Therefore, g_{m1}, r_{ds1}, and r_{ds3} should be increased to increase f_{3dB}. In the opposite case of $f_{3dB} >> f_{ca}$, A is presented by F/if where $F = A_0\, f_{ca}$ is the gain-bandwidth product of the amplifier and approximately the same as the cutoff frequency (f_T) of the composite FET. In this case $Z_t(f)$ is rewritten in the form

$$Z_t(f) = -R_f \,/\, (1 + if \,/\, F - f^2 \,/\, F\, f_{ci}). \qquad (4\text{-}12)$$

In this case the frequency dependence of Z_t has resonance and f_{3dB} is limited by f_{ci} and F. To increase f_{3dB}, f_T should be increased.

4-3. Fabrication

In this study, three types of photoreceivers have been fabricated, which are distinguished by the gate length of the composite FET's and the feedback resistance. The gate length is 6 μm for Type I, and 3 μm for Types II and III. The feedback resistance is 1.2 kΩ for Types I and II, and 3.6 kΩ for type III. Type I was fabricated for the first time. Types II and III have been fabricated to aim at higher-speed and higher-sensitivity operation, respectively.

The fabrication steps of the photoreceiver are illustrated in Fig. 4-5. To fabricate the photoreceiver, an n-InGaAsP layer (1.0 μm, 1×10^{16} cm^{-3}, bandgap wavelength $\lambda_g = 1.1$ μm), an n-InP layer (1.5 μm, 5×10^{17} cm^{-3}), and an n^--InGaAs layer (2.0 μm, 5×10^{15} cm^{-3}) are first grown by LPE on a semi-insulating InP substrate as shown in Fig. 4-5(a). Then the InGaAs layer, the InP layer, and the InGaAsP layer are etched successively to form the mesa shape in Fig. 4-5(b). The InGaAs and the InGaAsP layers are selectively etched by H_2SO_4:H_2O_2:H_2O (1:1:5 and 5:1:1 in volume) and the InP layer is by HCl:H_3PO_4 (1:4 in volume). Etching each

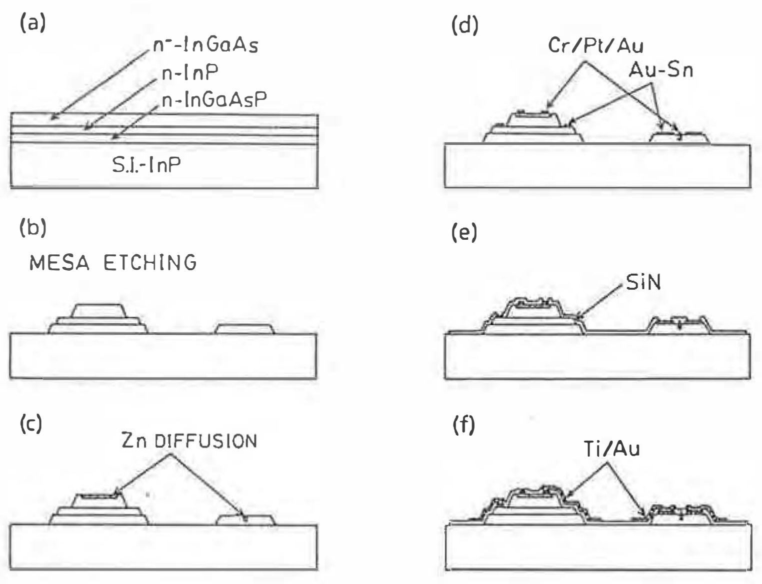


Fig. 4-5 Fabrication steps of the monolithic photoreceiver.

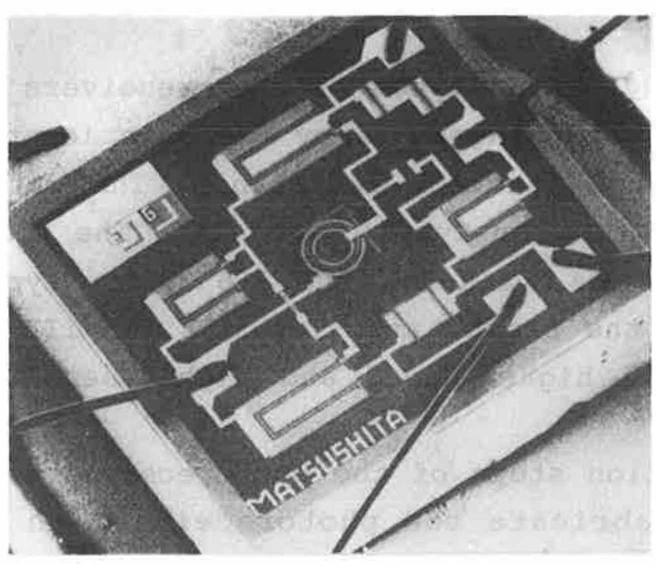
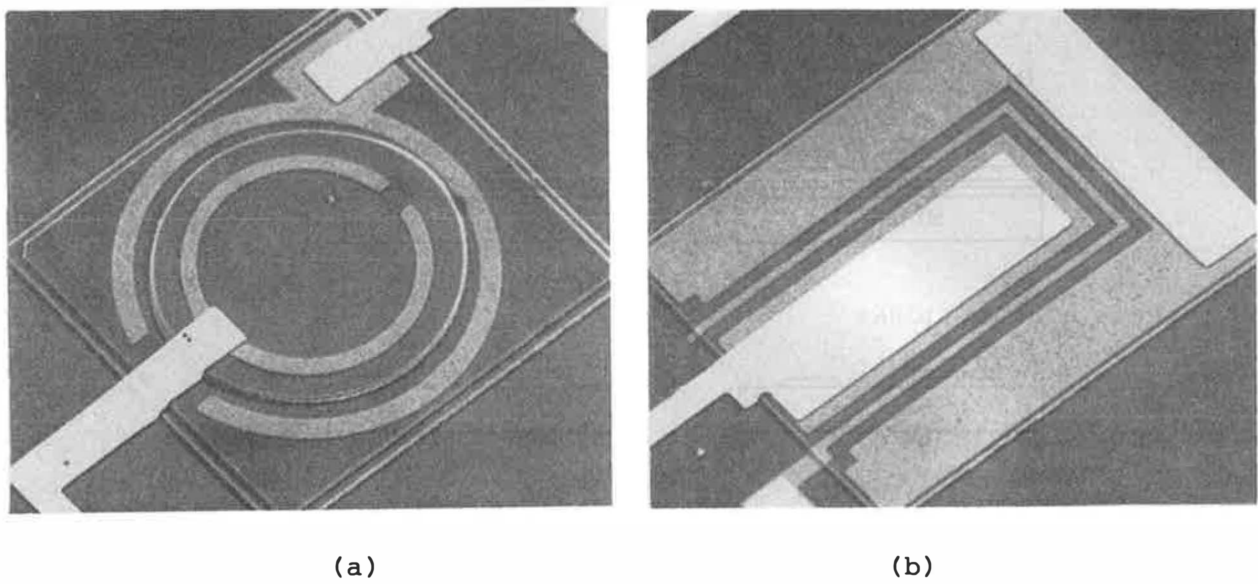


Fig. 4-6 SEM photograph of a fabricated photoreceiver. The chip size is 1.1 X 1.0 mm^2.

layer is easy and reproducible since preferential etchants are used. After the mesa formation, Zn is diffused into the PD, the gate of the FET's, and the p-type region of the level shift



(a) (b)

Fig. 4-7 SEM photographs of (a) a pin PD and (b) a junction FET. In the PD, inside of the ring anode corresponding to the photosensitive area has a diameter of 80 μm. The FET has a size of 260 X 150 μm^2.

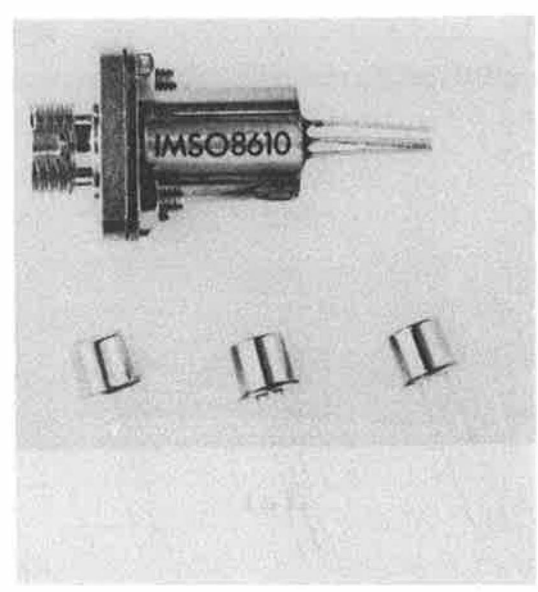


Fig. 4-8 Photomicrograph of assembled photoreceivers. The upper shows a receptacle type module for the FC connector. The lower is standard TO-18 packages.

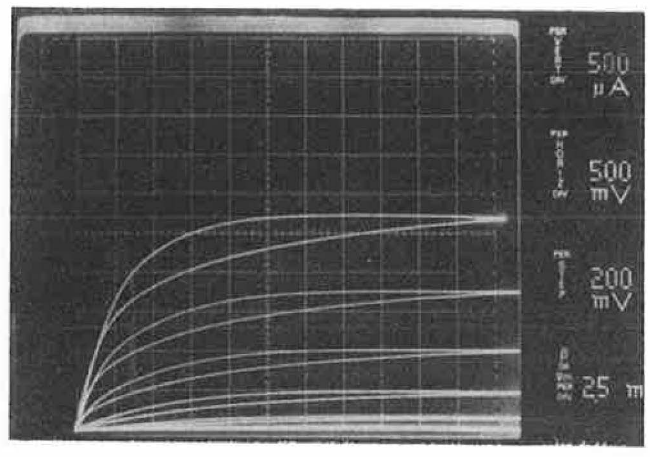
diodes in Fig. 4-5(c). Then Cr/Pt/Au and Au-Sn are evaporated as p-type and n-type ohmic contacts, respectively, in Fig. 4-5(d), and a SiN_x passivation film is deposited in Fig. 4-5(e). Finally Ti/Au interconnection metal is formed and connected to the contact metal through a window in the SiN_x film in Fig. 4-5(f).

An SEM photograph of the fabricated photoreceiver chip is shown in Fig. 4-6. The chip size is $1.1 \times 1.0\ mm^2$. The PD is located at the center of the chip to simplify the fiber coupling. The magnified photographs of the PD and the FET are shown in Fig. 4-7. No defects are observed in the interconnection metal pattern though the devices have mesa structures. The fabricated chip is mounted on a TO-18 package and assembled in a receptacle type module as shown in Fig. 4-8.

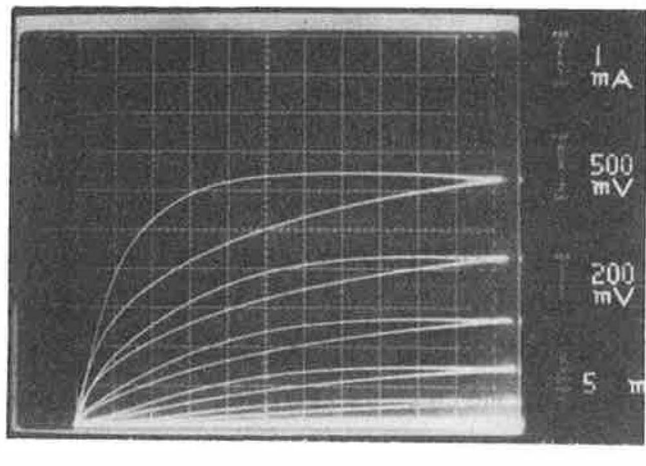
4-4. Characteristics of Composite Devices

4-4-1. General characteristics of FET's

The drain-source characteristics of a typical FET with a gate length of 6 μm and a width of 500 μm are shown in Fig. 4-9(a). The hysteresis loops observed in them are discussed in the following



(a)



(b)

Fig. 4-9 Drain- source voltage - current characteristics of typical FET's with gate lengths of (a) 6 μm and (b) 3 μm. Both FET's have a gate width of 500 μm.

section. The FET has a pinch-off voltage (V_{po}) of -1.0 V, a saturation drain current (I_{dss}) of 2.7 mA, and a transconductance (g_m) of 5.0 mS at zero gate bias. Frequency characteristics of S-parameters have been measured for another FET with the same gate length and width. The FET has V_{po} of -1.2 V, I_{dss} of 4.5 mA, and g_m of 7.0 mS. The current gain (h_{21}) derived from the measured S-parameters are plotted against frequency as shown in Fig. 4-10, from which a cutoff frequency (f_T) of 920 MHz is obtained. From

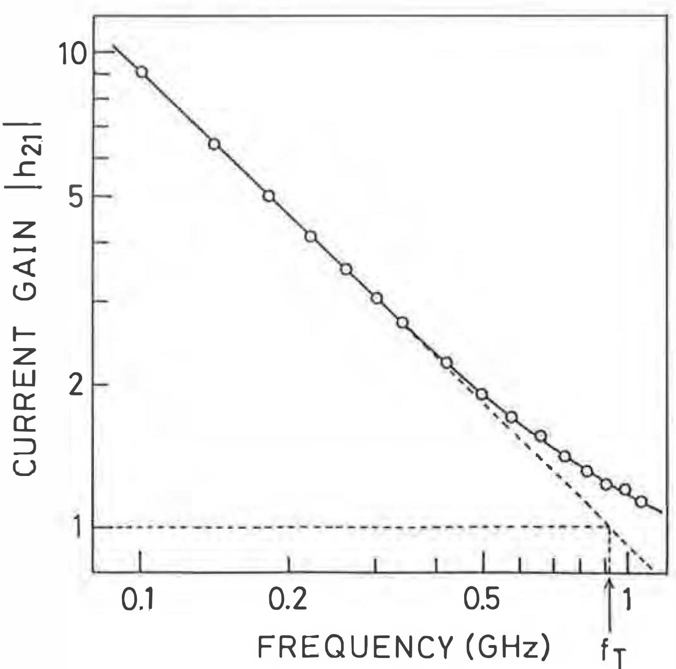


Fig. 4-10 Frequency characteristics of current gain for a FET with a gate length of 6 µm. The cutoff frequency (f_T) is 920 MHz.

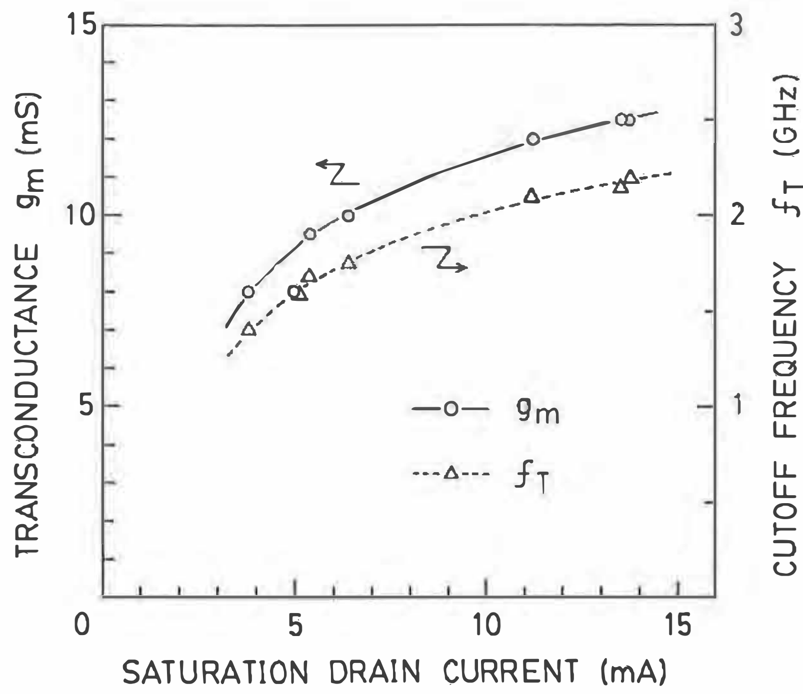


Fig. 4-11 Relation between saturation drain current and either transconductance or cutoff frequency for FET's with a gate length of 3 µm.

the value of g_m and f_T, the gate capacitance (C_g) is deduced to be 1.2 pF.

The drain-source characteristics of Fig. 4-9(b) have been measured for a FET with a gate length of 3 μm and a width of 500 μm. It has V_{po} of -1.1 V, I_{dss} of 6.4 mA, and g_m of 10 mS. The relation between I_{dss} and g_m for several FET's with different V_{po} is shown in Fig. 4-11. It coincides with the general relation that g_m is proportional to $I_{dss}^{1/2}$. The frequency characteristics of the same FET's have been measured. The obtained f_T are also plotted in Fig. 4-11. The f_T of the FET shown in Fig. 4-9(b) is 1.75 GHz. The proportional dependence of f_T on g_m represents the constant C_g which is calculated to be 0.91 pF.

4-4-2. Output resistance of FET's

The drain-source characteristics in Fig. 4-9 measured with a curve tracer (Type 576, Tektronix) exhibit hysteresis loops. These loops can be eliminated as shown in Fig. 4-12 by illuminating the FET's with a microscope lamp. Furthermore, the characteristics measured by DC mode without illumination has no hysteresis loops just like the AC characteristics under illumination. From these facts, the hysteresis loops are deduced to be caused by the slow traps which have time constant corresponding to the sweep

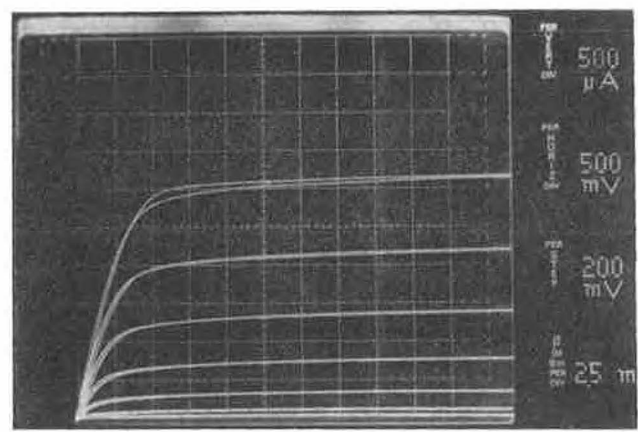


Fig. 4-12 Drain-source voltage-current characteristics of the FET shown in Fig. 4-9(a) under illumination with microscope lamp. The hysteresis loops are eliminated.

speed of curve tracer (60 Hz). Since further experiments revealed that the Fe doping level of the semi-insulating InP substrate affects the shape of the loop, the traps are thought to be associated with Fe and located at the interface between the Fe-doped InP substrate and the FET channel.

The hysteresis loops imply the change of output resistance (r_{ds}) of the saturation region in very low frequency range. Then the frequency dependence of r_{ds} has been measured in the frequency range from 1 Hz to 100 MHz. It was measured with an oscilloscope from 1 Hz to 1 MHz and with an impedance analyzer from 1 MHz to 100 MHz. The results are shown in Fig. 4-13 in which r_{ds} is drastically reduced in the frequency range from 10 Hz to 1 kHz and becomes constant above 100 kHz. The slight discontinuities at 1 MHz are attributed to the different methods of measurement. As can be seen from Fig. 4-13, the 3 μm gate FET has smaller r_{ds} than the 6 μm gate FET since the shorter gate shortens the current pass in the pinched channel which is the origin of finite r_{ds}. The relation between gate length and r_{ds} is thought to be approximately in-

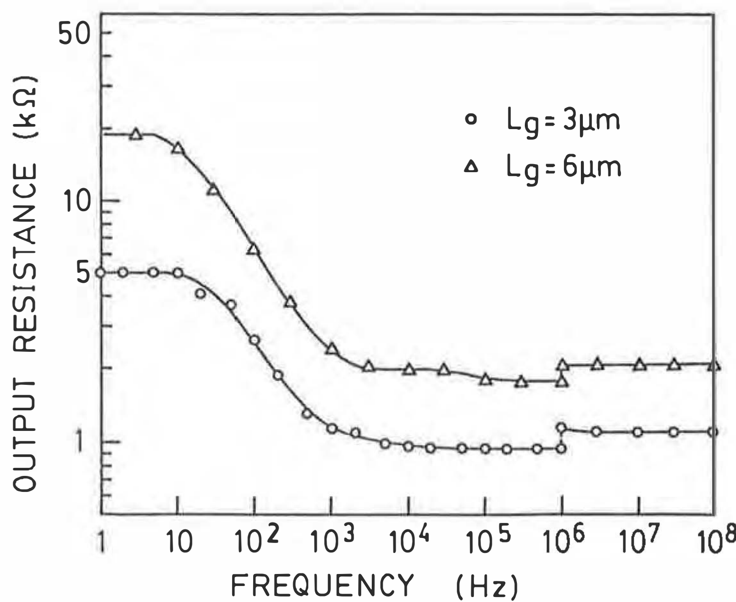


Fig. 4-13 Frequency dependence of drain - source output resistance in saturation region for FET's with gate lengths of 3 μm and 6 μm. The DC bias voltage applied to drain - source is 2.5 V.

verse proportion though exact analysis has not been done.

As described in Section 4-2-3, the product of $g_m r_{ds}$ is one of the important parameters which affect the frequency characteristics of transimpedance photoreceivers, because it decides the open loop gain of the preamplifier beneath cutoff frequency. For the photoreceivers fabricated in this study, the gain in the frequency range above 100 kHz is quite different from DC gain since r_{ds} is changed. Therefore, the low frequency gain (A_0) is defined as the gain in the frequency range above 100 kHz and beneath cutoff frequency. How A_0 affects the frequency characteristics of the photoreceivers is discussed in Section 4-7-1.

4-4-3. Characteristics of PD's

Dark currents of several PD's have been measured in relation to the reverse bias voltage. The result for the PD with the lowest dark current is shown in Fig. 4-14. This PD has a dark current of 30 nA at a bias voltage of -3 V, which is the operating voltage in the integrated circuit. The typical values of dark current at -3 V are a few μA. This rather large dark current is

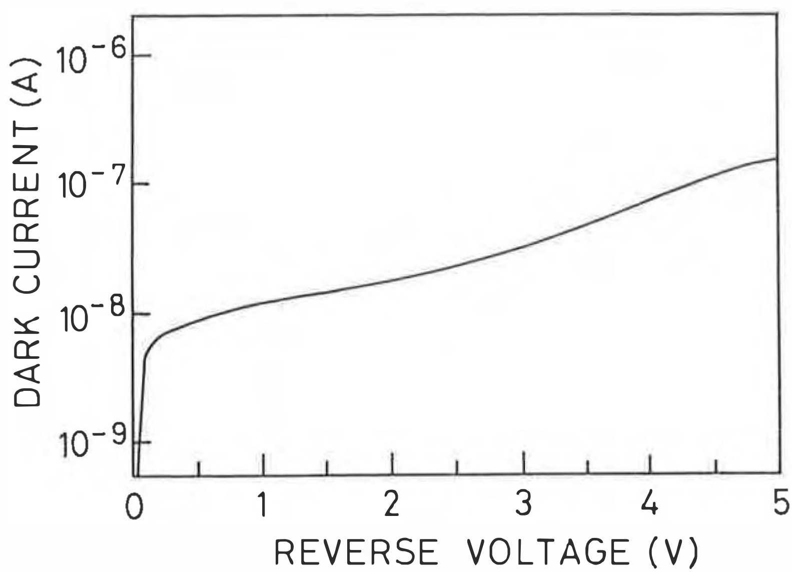


Fig. 4-14 Relation of reverse voltage and dark current for the PD with the lowest dark current among measured samples.

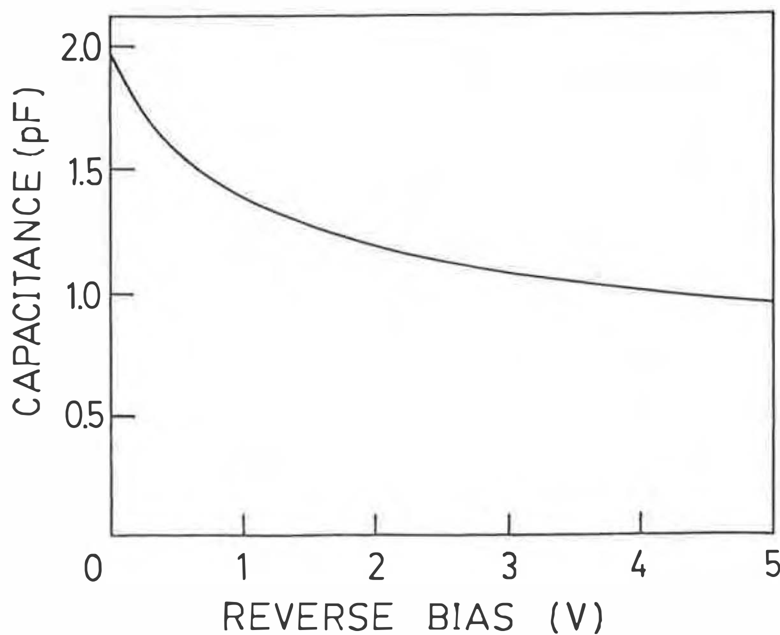


Fig. 4-15 Relation of reverse voltage and capacitance for a typical PD.

attributed to the SiN_x passivation film [4]. However, it should be noted that the shot noise induced by dark current of a few μA is still smaller than the thermal noise of the feedback resistor.

The capacitance of PD has also been measured by changing bias voltage as shown in Fig. 4-15. The value at a bias voltage of -3 V is 1.1 pF. Since the capacitance of the interconnection metal across the n-type region is about 0.1 pF, the junction capacitance of the PD is about 1.0 pF, from which the carrier concentration of the n^--InGaAs layer is deduced to be 7×10^{15} cm^{-3}.

4-5. Circuit Characteristics

4-5-1. Circuit operation

The circuit operation of the Type I photoreceiver has first been examined. It has a gate length of 6 μm and a feedback resistor of 1.2 kΩ. A 1.3 μm laser diode with a fiber pigtail was used as an optical source. The end of the pigtail was butted to the photoreceiver. The quantum efficiency of the photodiode is 70% or

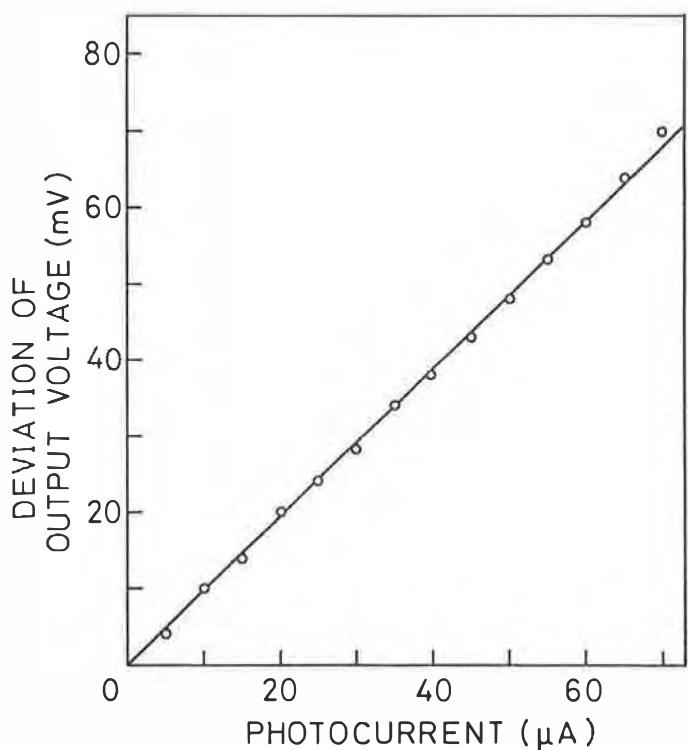


Fig. 4-16 Relation between photocurrent and change in output voltage for a Type I photoreceiver having a gate length of 6 μm and a feedback resistor of 1.2 kΩ.

more without correction for coupling loss. The relation between the photocurrent and the change in output voltage is shown in Fig. 4-16. The measured transimpedance is 965 Ω which is thought to be approximately the same as feedback resistance.

The frequency characteristics have also been measured by modulating the laser diode. In this measurement, bypass capacitors were inserted in parallel to the level shift diodes to improve the frequency characteristics of the diodes. An emitter follower circuit was used to transform output impedance because the photoreceiver has a rather high output impedance of 200 Ω. The measured characteristics are shown in Fig. 4-17. The 3dB bandwidth (f_{3dB}) of the photoreceiver is 240 MHz. Both the static and high-frequency characteristics show that this photoreceiver can operate normally with a 5 V power supply.

However, it should be pointed out that the transimpedance

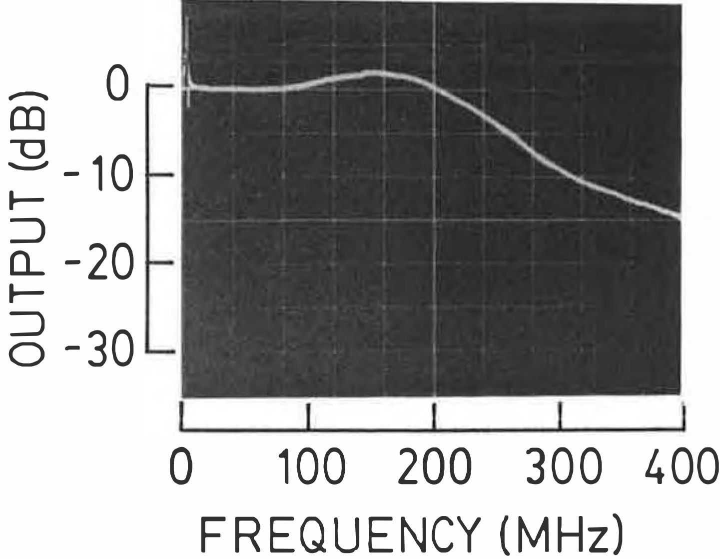


Fig. 4-17 Frequency response of a Type I photoreceiver. The 3 dB bandwidth is 240 MHz.

corresponding to the 0 dB line in Fig. 4-17 is different from the DC transimpedance obtained from Fig. 4-16. As described in Section 4-4-2, the amplifier gain in the frequency range between 100 kHz and cutoff frequency is smaller than DC gain since the output resistance of FET's are reduced. Therefore, the low-frequency transimpedance in the frequency range between 100 kHz and f_{3dB} is also smaller than DC transimpedance. The low-frequency transimpedance (at 10 MHz) has been measured to be 750 Ω for the photoreceiver with a DC transimpedance of 1.13 kΩ.

4-5-2. Dissipation current and bandwidth

The speed of the photoreceivers depend on drain current of the FET's since g_m, f_T, and r_{ds} depend on it. The drain current for each FET is a half of the total dissipation current (I_d) since the FET's Q3 and Q4 shown in Fig. 4-1 have the same gate size. The relations between I_d and f_{3dB} are shown in Fig. 4-18 for Types I and II photoreceivers. Type II with a gate length of 3 μm has been fabricated for higher speed operation. The supply voltage for photoreceivers are fixed to 5 V. The frequency response of the Type II photoreceiver with the highest f_{3dB} of 285 MHz is

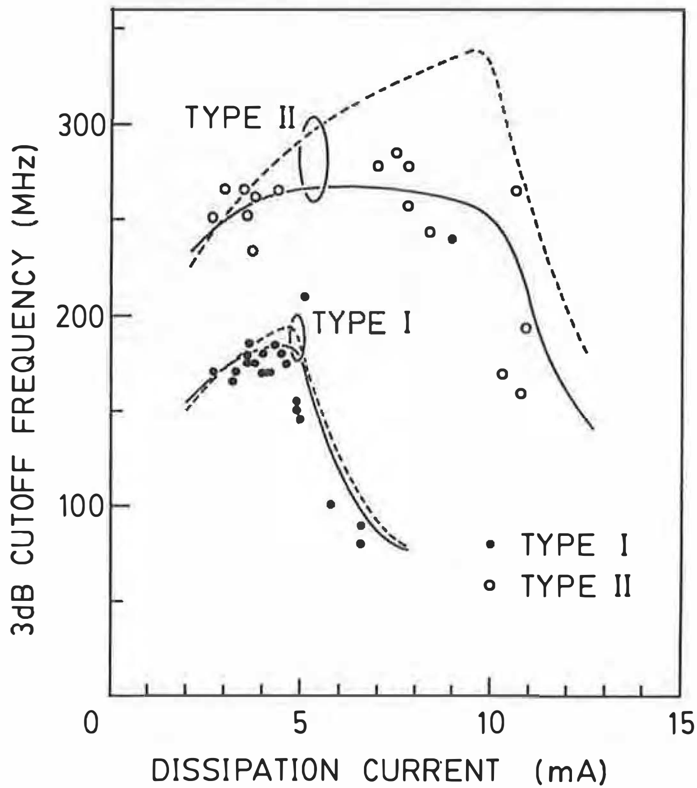


Fig. 4-18 Relation between dissipation current and 3 dB bandwidth for Types I and II photoreceivers. The solid lines shows results of computer circuit simulation with device parameters shown in Table 4-2. The broken lines are results obtained on the assumption that output resistance in saturation region is infinite.

shown in Fig. 4-19.

The solid lines in Fig. 4-18 show results of computer circuit simulation. The device parameters for simulation are determined by the measured value as listed in Table 4-2. The broken lines also show results of simulation using the same parameters except that r_{ds} in the saturation region is infinite. For Type I photoreceivers, the solid and the broken lines show quite small difference, which means the finite r_{ds} does not affect the frequency characteristics. For Type II photoreceivers, however, the solid and the broken lines show difference in the high I_d region, and the measured values correspond to solid lines. Therefore, the speed of Type II photoreceivers is thought to be limited by A_0 in

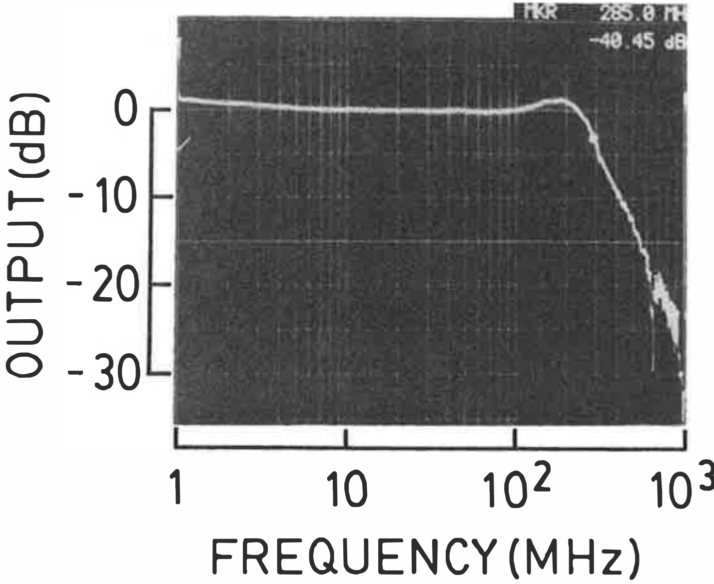


Fig. 4-19 Frequency response of the Type II photoreceiver with the highest 3dB bandwidth of 285 MHz. The Type II photoreceiver has a gate length of 3 μm and a feedback resistance of 1.2 kΩ.

Table 4-2 Parameters of the FET and other devices used for the computer circuit simulation.

PARAMETER	Type I	Type II	Type III
TRANSCONDUCTANCE PARAMETER (g_m / $2\|V_{po}\|$) (mA/V^2)	2.5	4.5	4.5
GATE CAPACITANCE (pF)	1.2	0.9	0.9
OUTPUT RESISTANCE PARAMETER (1 / $r_{ds}I_{dss}$) (1/V)	0.13	0.17	0.17
FEEDBACK RESISTANCE (kΩ)	1.2	1.2	3.6
PHOTODIODE CAPACITANCE (pF)	1.1	1.1	1.1
SUPPLY VOLTAGE (V)	5.0	5.0	5.0

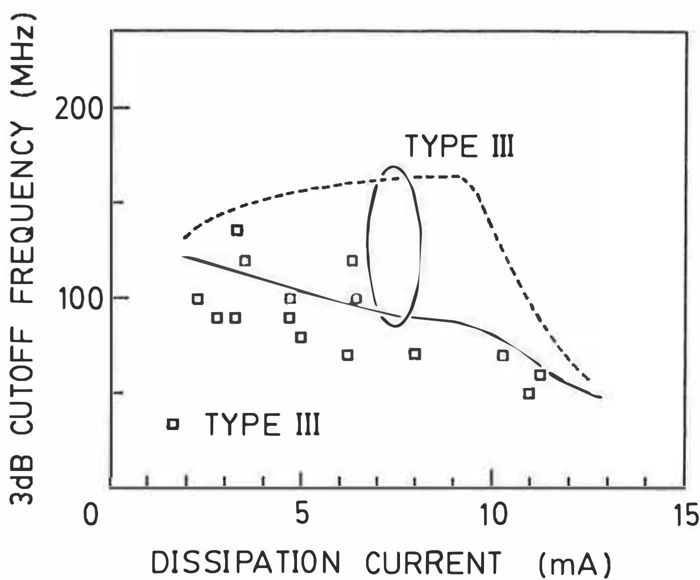


Fig. 4-20 Relation between dissipation current and 3 dB bandwidth for Type III photoreceivers. The solid and the broken lines have the same meaning as the lines in Fig. 4-18.

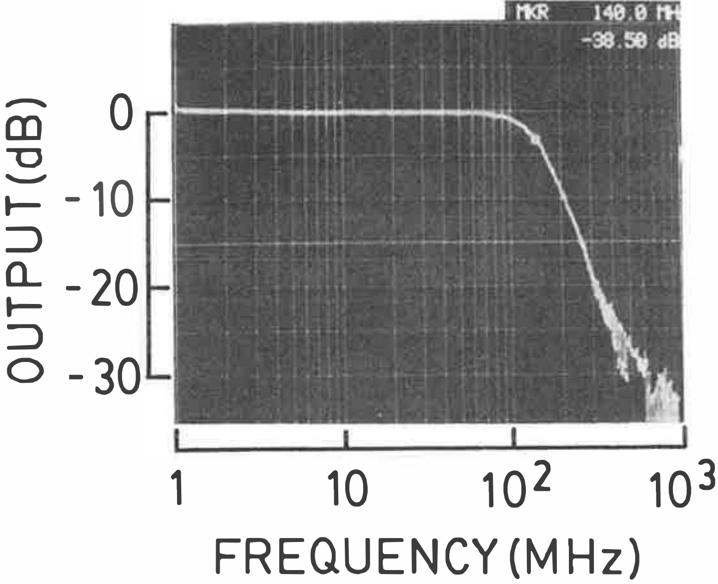


Fig. 4-21 Frequency response of the Type III photoreceiver with the highest 3dB bandwidth of 140 MHz. The Type III photoreceiver has a gate length of 3 μm and a feedback resistance of 3.6 kΩ.

high I_d region.

Type III photoreceivers, which have a gate length of 3 μm and a feedback resistance of 3.6 kΩ, are aimed at higher sensitivity. The relation between I_d and f_{3dB} for Type III photoreceivers is shown in Fig. 4-20. The frequency response of the Type III photoreceiver with the highest f_{3dB} of 140 MHz is shown in Fig. 4-21. The solid and broken lines in Fig. 4-20 have the same meaning as the lines in Fig. 4-18. For Type III photoreceivers, the solid and the broken lines show difference not only in high I_d region but also in low I_d region. Therefore, the speed of Type III photoreceivers are thought to be limited by A_0 over the full I_d range.

4-5-3. Transmission characteristics

The transmission characteristics have been measured by modulating the optical source with a non-return-to-zero (NRZ) pseudorandom bit sequence. The output signal of the external emitter follower circuit was first observed with oscilloscope to obtain eye pattern. The eye pattern at 400 Mbit/s for the Type I photoreceiver with f_{3dB} of 240 MHz is shown in Fig. 4-22. The rise and the fall times are approximately 1.8 ns which corresponds to the

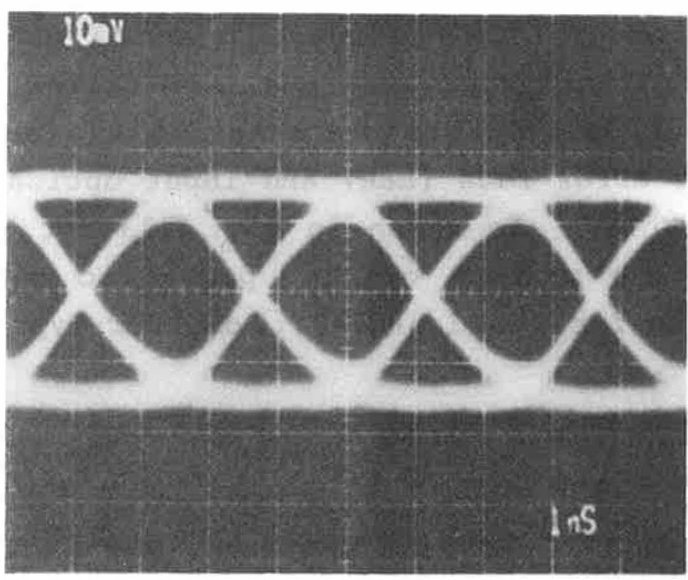


Fig. 4-22 Eye pattern obtained by using a Type I photoreceiver for 400 Mbit/s non-return-to-zero pseudorandom bit sequence.

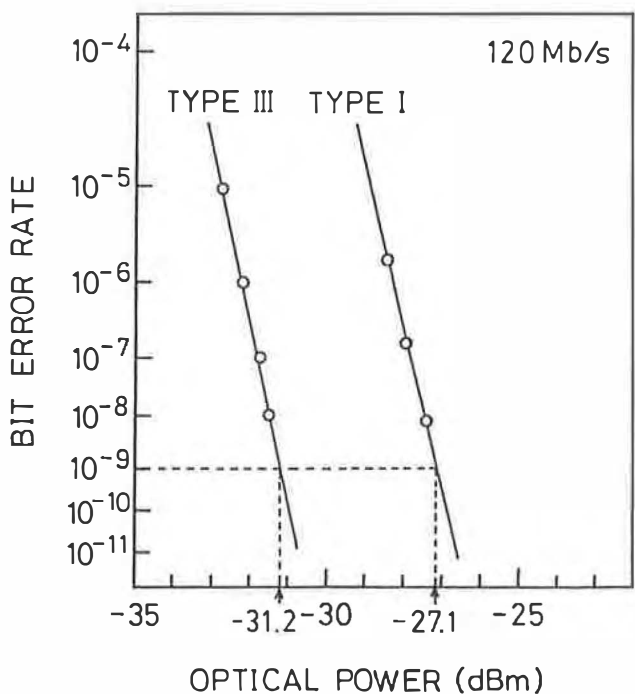


Fig. 4-23 Bit error rate (BER) against input optical power measured at a bit rate of 120 Mbit/s. The minimum optical powers to obtain a BER of 10^{-9} are -27.1 dBm for Type I and -31.2 dBm for Type III.

value derived from f_{3dB}.

Then the bit error rate has been evaluated with an automatic gain control (AGC) amplifier, an equalizer filter, a discriminator, and an error detector to characterize the sensitivity. The relations of bit error rate (BER) and input optical power at the bit rate of 120 Mbit/s are shown in Fig. 4-23 for Types I and III photoreceivers. The minimum optical powers to obtain a BER of 10^{-9} are -27.1 dBm for Type I and -31.2 dBm for Type III.

4-6. Photoreceiver with Self-Aligned FET's

4-6-1. Device structures

As described in the previous sections, the photoreceiver with a shorter gate length has higher operation speed. However, it is difficult to fabricate an FET with a gate length shorter than 3 μm since some margins are required for the alignment of the

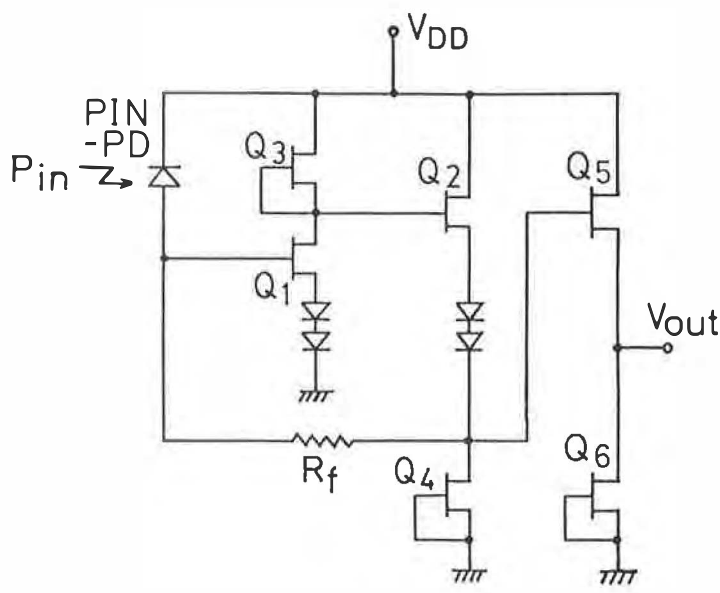


Fig. 4-24 Circuit diagram of the photoreceiver with self-aligned FET's.

gate metal and the gate diffused area. To obtain shorter gate length, it is favorable to adopt a self-aligned gate structure. The junction FET with a self-aligned gate has been fabricated easily by using the gate metal as an etching mask for the p-type gate on the n-type channel [13-15]. Crystals with different compositions are grown as the gate and the channel layers which enable one to use preferential etchants for etching only the gate. The overhang of the gate metal formed with side etching of the gate layer is used for mask-less self-aligned evaporation of source and drain metals.

In this study, the photoreceivers incorporating the self-aligned junction FET's described above have been fabricated to improve the bandwidth. The device structures are the same as the structure shown in Fig. 4-1 except that the n-InGaAsP channel is separated to a p-InGaAsP gate and an n-InP channel, and that the FET has a self-aligned structure. In regard to the circuit configuration, an output buffer stage has been added to the conventional circuit as shown in Fig. 4-24. The roles of this buffer stage are to reduce output impedance and to prevent the output

load capacitance from affecting the feedback circuit.

4-6-2. Fabrication

To fabricate the photoreceiver with self-aligned FET, an n-InP channel layer (0.5 μm, 1×10^{16} cm^{-3}), a p-InGaAsP gate layer (0.5 μm, 5×10^{17} cm^{-3}, bandgap wavelength $\lambda_g = 1.1$ μm), an n-InP layer (1.5 μm, 5×10^{17} cm^{-3}), and an n^--InGaAs layer (2.0 μm, 5×10^{15} cm^{-3}) are first grown by LPE on a semi-insulating InP substrate. Then the InGaAs layer and the upper InP layer are etched successively to form the mesa shape. After the mesa formation, Zn is diffused into the PD. Then Cr/Pt/Au are evaporated to form the anode of PD and the gate metal of FET, and the gate layer is etched by using the gate metal as a etching mask. After evaporation of Au-Sn for n-type ohmic contacts, a SiN_x passivation film is deposited. Finally Ti/Au interconnection metal is formed and connected to the contact metal through a window in the SiN_x.

An SEM photograph of the fabricated photoreceiver chip is shown in Fig. 4-25. The chip size is 1.0 X 0.9 mm^2. The PD has a diffused area of 40 μm and a photosensitive area of 20 μm which is

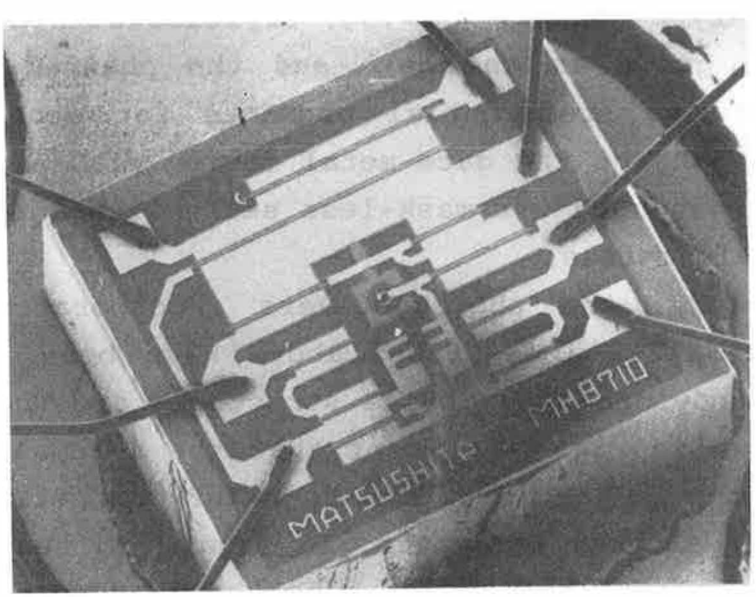


Fig. 4-25 SEM photograph of a fabricated photoreceiver with self-aligned FET's. The chip size is 1.0 X 0.9 mm^2.

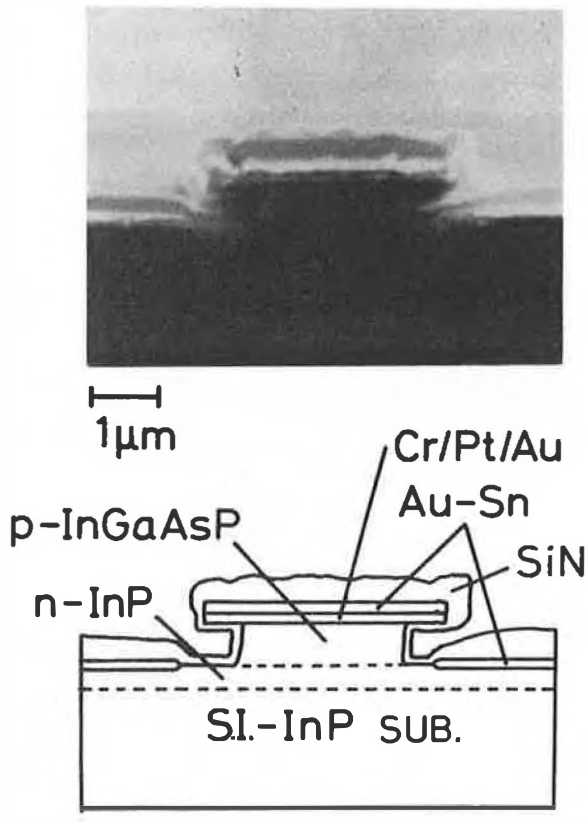


Fig. 4-26 Cross-sectional SEM photograph of a self-aligned gate structure.

designed by considering the coupling with a single mode fiber. A cross-sectional SEM photograph of the self-aligned gate is shown in Fig. 4-26. The gate length is 2.5 µm and the distances between gate-source and gate-drain are 0.2 µm and 0.8 µm, respectively.

4-6-3. Characteristics of FET's

The drain-source characteristics of a self-aligned FET with a gate width of 200 µm are shown in Fig. 4-27. It has a pinch-off voltage (V_{po}) of -2.0 V, a saturation drain current (I_{dss}) of 8.0 mA, and a transconductance (g_m) of 6.0 mS (30.0 mS/mm) at zero gate bias. The frequency dependence of current gain derived from the S-parameters is shown in Fig. 4-28. A cutoff frequency (f_T) of 3.0 GHz is obtained.

The values of g_m and f_T have been improved compared with the conventional 3 µm-gate FET with the same V_{po}. The conventional FET

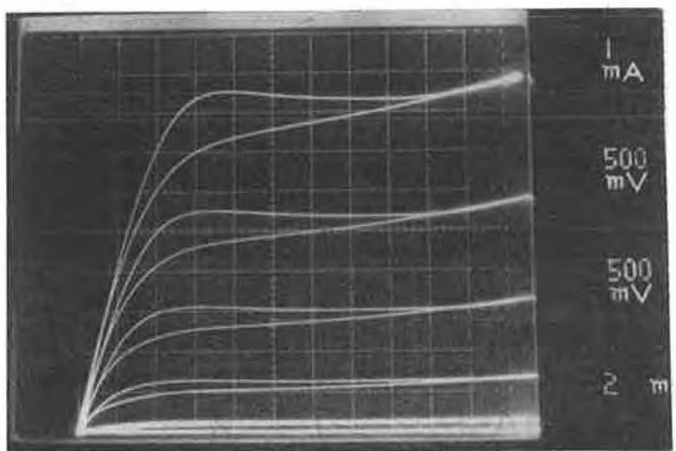


Fig. 4-27 Drain-source voltage-current characteristics of a typical FET with a self-aligned gate. The FET has a gate length of 2.5 μm and a gate width of 200 μm.

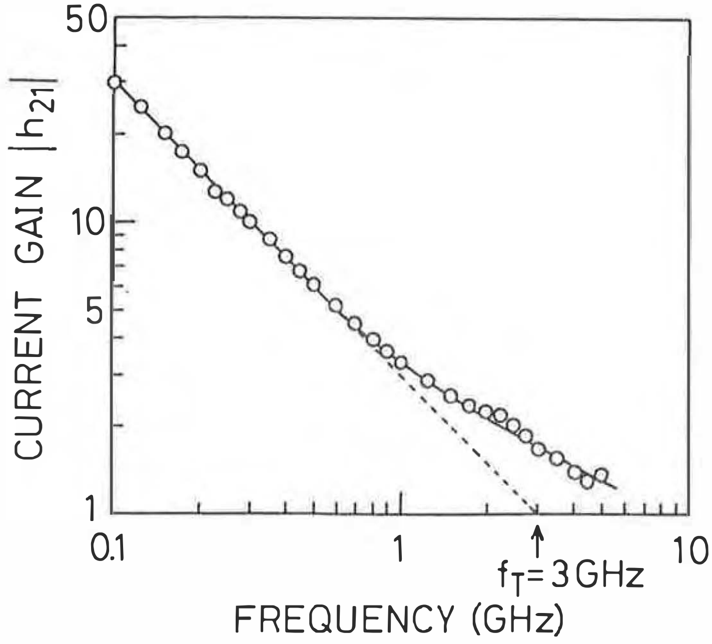


Fig. 4-28 Frequency characteristics of current gain for a FET with a self-aligned gate. The cutoff frequency (f_T) is 3.0 GHz.

has g_m of 12.5 mS (25.0 mS/mm) and f_T of 2.2 GHz. These improvements correspond to the reduction rate of gate length since g_m and f_T are proportional to the gate length and its square, respectively. To obtain more drastic improvements, further reduction of the gate length is necessary.

4-6-4. Circuit characteristics

The frequency response of a fabricated photoreceiver is shown in Fig. 4-29. The 3 dB bandwidth (f_{3dB}) is 360 MHz. This result was obtained using a power supply voltage of 7 V. In case of operating it with a 5 V power supply both the transimpedance in low frequency range and f_{3dB} were decreased.

Considering reduction of the PD capacitance, operation speed of this photoreceiver is inferior to the conventional photoreceivers. This is because $|V_{po}|$ of FET was too large and the DC bias point was in linear region. For the conventional FET, the channel depth determining V_{po} is controlled by gate diffusion. However, the channel depth of the self-aligned FET is equal to

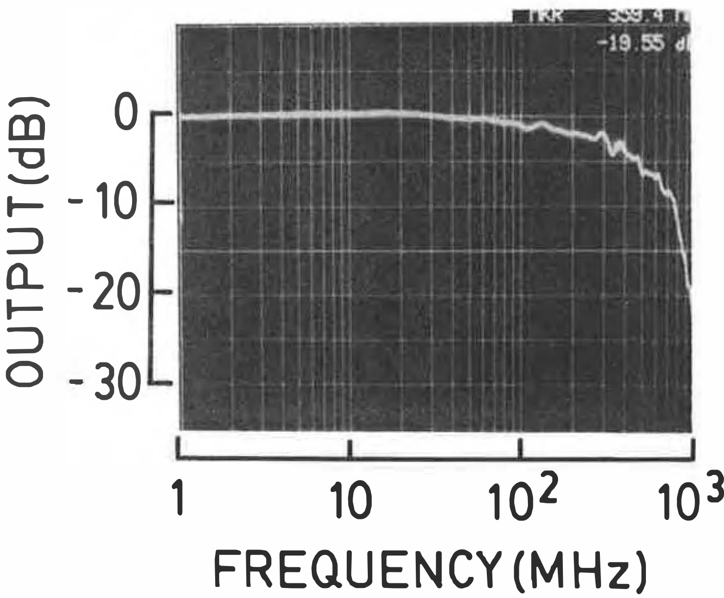


Fig. 4-29 Frequency response of a photoreceiver with self-aligned FET's. The 3 dB bandwidth is 360 MHz.

the channel layer thickness. As a result, the control of channel depth is very difficult for the self-aligned FET due to uncertainty of layer thickness grown by LPE.

4-7. Approach to a photoreceiver grown by OMVPE

4-7-1. Device structures

One way to improve the controllability of channel depth for the self-aligned FET is utilizing OMVPE for epitaxial growth. Furthermore, OMVPE has two additional advantages, which are the growth of InP on InGaAs and the growth on substrate with mesa-shape structures. Based on these advantages of OMVPE, a new integrated structure shown in Fig. 4-30 has been proposed [16].

In this structure, the PD is constructed with an n^--InGaAs and an n-InGaAsP layers grown by LPE, and an n-InP window layer grown by OMVPE. The InP window layer is effective to reduce the dark current of the PD. The n-InP window layer is used as a channel layer in the FET which is grown directly on a semi-insulating InP substrate outside of the PD region. The self-aligned FET is constructed with this channel layer and a p-InGaAsP gate layer grown by OMVPE. These layer structures are formed by LPE and OMVPE with mesa etching after each epitaxial growth.

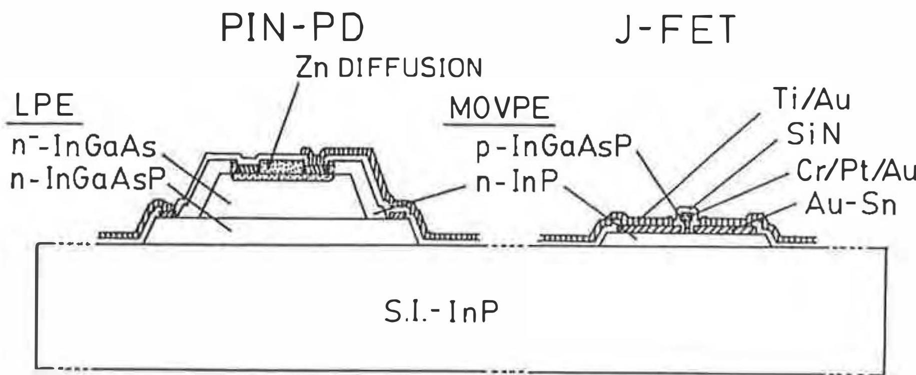


Fig. 4-30 Schematic cross-section of the photoreceiver grown by OMVPE.

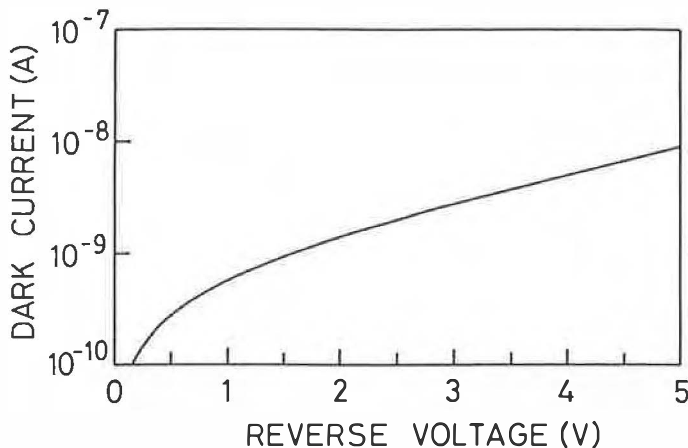


Fig. 4-31 Relation of reverse voltage and dark current for a typical PD with a window layer grown by OMVPE.

4-7-2. PD with a window layer

For the first stage of developing the integrated structure shown in Fig. 4-30, a PD with a window layer grown by OMVPE has been fabricated. To fabricate the PD, an n-InGaAsP and an n^--InGaAs are first grown by LPE. Then they are etched with preferential etchants to leave the mesa shape. After mesa formation, the window layer is grown by OMVPE. After the second growth, Zn is diffused to form the p-type region, and Cr/Pt/Au and Au-Sn were evaporated for the anode and the cathode, respectively. To reduce the contact resistance, the anode of the PD was formed after etching the window layer beneath it.

Typical dark current of the PD with a diffusion area of 100 μmϕ is shown in Fig. 4-31 in relation to the bias voltage. The dark current at the bias voltage of -3 V is 2.7 nA. this value is much smaller than dark current of the PD without a window layer which ranged from 30 nA to a few μA. This result showed that the InP layer grown by OMVPE on an InGaAs mesa had enough quality as a window layer.

4-7-3. Self-aligned FET

The self-aligned FET has been fabricated by using the channel

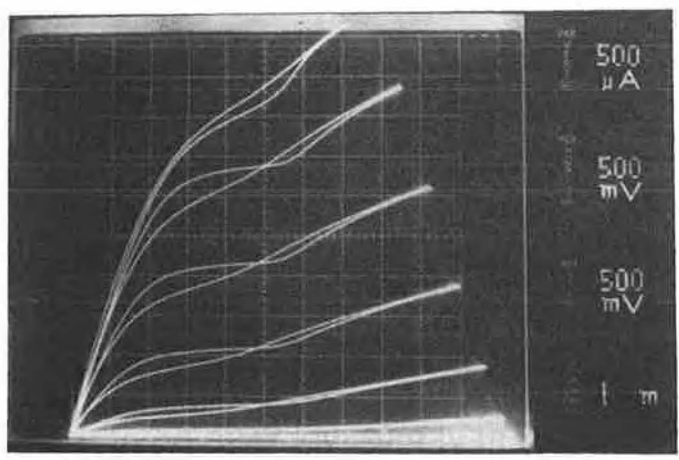


Fig. 4-32 Drain-source voltage-current characteristics of a typical FET grown by OMVPE with a self-aligned gate. The FET has a gate length of 2.5 μm and a gate width of 200 μm.

and the gate layers grown by OMVPE. The fabrication steps are the same as those of the self-aligned FET grown by LPE. The drain-source characteristics of a fabricated FET with a gate width of 200 μm are shown in Fig. 4-32. This FET has V_{po} of -2.5 V, I_{dss} of 4.3 mA, and the maximum g_m of 2.4 mS. The value of g_m is much smaller than the FET grown by LPE and maximum g_m is not obtained at zero gate bias.

These results are thought to be caused by traps in the channel layer grown by OMVPE. For the FET described above, the carrier concentration of the channel layer obtained from the sheet resistance was 6×10^{15} cm^{-3}, while the donor density from the capacitance was 7×10^{16} cm^{-3}. This discrepancy shows that the neutral electron traps compensate carriers. The traps capture electrons and has negative charge in thermal equilibrium, and they emit electrons and are neutral in the depletion layer.

Due to these traps, the depletion layer thickness is less controllable by the gate bias voltage, and less carriers flow through the conductive channel compared with the channel layer grown by LPE. The LPE-grown channel has a carrier concentration of 1×10^{16} cm^{-3} and approximately the same donor density. Therefore, g_m of FET grown by OMVPE is smaller than that by LPE. The

reason why maximum g_m is not obtained at zero gate bias is attributed to the non-uniform distribution of the traps.

The origin of traps in epitaxial layers grown by OMVPE has not been clarified. Since the characteristics of FET are not improved until this problem is solved, the proposed structure shown in Fig. 4-30 has not been fabricated.

4-8. Discussion

4-8-1. Analysis for bandwidth

In this section, the limitation factors of the bandwidth are discussed for the Types I, II, and III photoreceiver demonstrated in Section 4-5. As shown in Figs. 18 and 20, the measured values of f_{3dB} coincide with the results of computer circuit simulation. By using the theory on the bandwidth of the transimpedance amplifier described in Section 4-2-3, the dependence of f_{3dB} on I_d shown in Fig. 18 or 20 is explained as follows. In high I_d region, the bias point of the FET moves into linear region and r_{ds} is decreased unrelated to the value in saturation region. Then f_{3dB} is limited by A_0 and decreased rapidly. This rapid decrease of f_{3dB} is observed for all of three types though the value of I_d where it starts is different. This difference is attributed to the different I_{dss} under the same V_{po} condition.

As for Type I photoreceivers f_{3dB} in low I_d region is limited by F since it is not affected by the value of r_{ds} in saturation region. Therefore, f_{3dB} is larger than f_{ca} in this case. It is increased with I_d since f_T increases in proportion to $I_d^{1/2}$. On the other hand f_{3dB} of Type III photoreceivers in low I_d region is limited by A_0 determined by r_{ds} in saturation region. In this case f_{3dB} is smaller than f_{ca} since shortened gate length increases f_{ca} and increased R_f decreases f_{3dB}. Increment of I_d decreases f_{3dB}, because r_{ds} decreases in inverse proportion to I_d while g_m increases in proportion to $I_d^{1/2}$. Type II photoreceivers have three factors which limit f_{3dB} according to I_d. They are F, A_0 determined by r_{ds} in saturation region, and A_0 determined by r_{ds} in linear region.

To consider the relation of the gate length and speed, A_0 and

f_{ci} for Types I and II have been calculated from the values listed in table 4-2. Assuming V_{po} = -1.0 V, A_0 for Types I and II are calculated to be 7.7 and 5.9, respectively. This result shows that shorter gate length decreases A_0 since the decrease of r_{ds} is more effective than the increase of g_m. Furthermore, the value of $(1 + A_0) f_{ci}$ for Type II is smaller than that of Type I since the increase of f_{ci} caused by the decrease of C_{gs} is less significant than the decrease of A_0. Therefore, shortening the gate length will decrease f_{3dB} in case that f_{3dB} is limited by A_0.

However, this result does not mean that the photoreceiver with self-aligned FET's demonstrated in Section 4-6 should have smaller f_{3dB} than Type II photoreceiver. For the photoreceiver with self-aligned FET's, the capacitance of the PD is also reduced by shrinking the photosensitive area. Therefore, the limitation factor of the bandwidth becomes F when the gate length is 3 µm, and shortening the gate length is favorable to increase f_{3dB}. According to the computer circuit simulation, the photoreceiver with self-aligned FET's is expected to have f_{3dB} of 900 MHz if the FET's has V_{po} of -1.0 V.

4-8-2. Analysis for sensitivity

To find the dominant noise source which limits the sensitivity of the photoreceiver, the output noise voltage has been measured for Type I photoreceiver with a spectrum analyzer after amplification by a broad-band amplifier. The measured noise voltage is shown in Fig. 4-33 accompanied by an equivalent input noise voltage of the FET which was calculated from the output noise of a gate-grounded source follower circuit.

As seen in Fig. 4-33, the dominant noise source of the photoreceiver between 1 MHz and 100 MHz is 1/f noise. The output noise of the photoreceiver corresponds to the input noise of the FET. This result shows that the 1/f noise of the FET is the dominant noise source of the photoreceiver because in a transimpedance circuit the input noise voltage of the amplifier appears at the output after multiplication by $A / (1 + A)$ where A is the open loop gain of the amplifier.

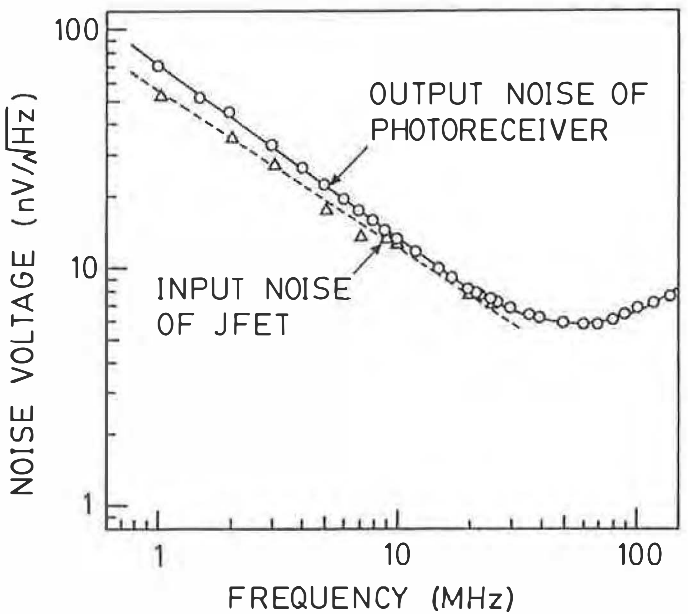


Fig. 4-33 Frequency dependence of output noise voltage for a Type I photoreceiver and input noise voltage for an FET with a gate length of 6 μm. The dominant noise source of the photoreceiver is 1/f noise generated in the FET.

In regard to sensitivity, the gate length does not affect noise characteristics in the frequency range less than 100MHz. The equivalent input noise current of Type I averaged in the frequency range from 1 MHz to 100 MHz varies from 12.6 $pA/\sqrt{Hz}$ to 41.1 $pA/\sqrt{Hz}$ with the magnitude of the 1/f noise, while thermal noise of the feedback resistor is a constant value of 4.4 $pA/\sqrt{Hz}$. The sensitivity data shown in Fig. 4-23 has been obtained for the photoreceiver with the lowest noise current. Type II has the same noise components and the same noise current distribution as Type I. Therefore, shortening the gate length does not affect the sensitivity at a bit rate of 120 MHz.

On the other hand, increasing the feedback resistor reduces the input noise current caused by the 1/f noise in inverse proportion to R_f since 1/f noise of FET can be treated as a noise voltage source at the gate. Therefore, Type III photoreceivers should have 4.8 dB better sensitivity than Type I or II if only the

1/f noise is considered. The thermal noise is, however, inversely proportional to $R_f^{1/2}$ and becomes comparable to the 1/f noise for the Type III receivers with low 1/f noise. In case of accounting both the 1/f noise and the thermal noise, the improvement of sensitivity is calculated to be 4.3 dB which corresponds to the result shown in Fig. 4-23.

4.8 Summary

In this chapter, the integration of a pin photodiode and an amplifier circuit was described. It is very attractive for high speed and low noise operation since the integration can reduce the front-end capacitance. The monolithic photoreceiver incorporating a pin photodiode (PD), four junction field effect transistors (FET's), four level shift diodes, and a feedback resistor has been designed and fabricated successfully. Both the static and the high-frequency characteristics shows that the photoreceiver operates normally with a single 5 V power supply.

The bandwidth has been measured in relation to the dissipation current for three types of photoreceivers which are distinguished by the gate length and the feedback resistance. The experimental results are well explained by theoretical considerations and coincide with the results of computer circuit simulation. Transmission characteristics have been measured to evaluate the sensitivity. It is limited by the 1/f noise of the front-end FET and has been improved by increasing the feedback resistance.

For higher speed operation, the photoreceiver with self-aligned gate FET's has been fabricated by using LPE. The bandwidth of the photoreceiver was inferior to the expected value since the pinch-off voltage of the FET's was larger than the designed value. The photoreceiver grown by OMVPE has been proposed for precise control of the pinch-off voltage. However, the self-aligned FET grown by OMVPE has much lower g_m than the FET by LPE. It is thought that there are neutral electron traps in the OMVPE-grown channel, which capture the carriers and reduce the drain-source current.

The important quantitative results obtained in this chapter

are as follows:

1) The FET with a gate length of 6 μm has a transconductance of 14.0 mS/mm and a cut-off frequency of 920 MHz, and the FET with a gate length of 3 μm has those of 20.0 mS/mm and 1.75 GHz.
2) The output resistance of the FET is drastically reduced in the frequency range from 10 Hz to 1 kHz and becomes constant above 100 kHz. This phenomenon is thought to be caused by the slow traps located at the interface between the Fe-doped InP substrate and the FET channel.
3) The highest 3 dB bandwidth of 285 MHz has been obtained for the photoreceiver with a gate length of 3 μm and a feedback resistance of 1.2 kΩ.
4) The minimum optical power to obtain a BER of 10^{-9} at the bit rate of 120 Mbit/s is -27.1 dBm for the photoreceiver with a feedback resistance of 1.2 kΩ and -31.2 dBm for that of 3.6 kΩ.
5) The maximum bandwidth of the photoreceiver with self-aligned gate FET's is 360 MHz. The computer circuit simulation shows that it will be improved to 900 MHz if the pinch-off voltage of the FET's are precisely controlled.

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V. INTEGRATION OF OPTOELECTRONIC BISTABLE SWITCHES
— PHOTONIC PARALLEL MEMORY (PPM) —

5-1. Introduction

In this chapter, a two-dimensional array of optoelectronic bistable switches is described, which is named a photonic parallel memory (PPM) [1,2]. The optoelectronic bistable switch in the PPM is an OEID consisting of a light emitting diode (LED) and a heterojunction phototransistor (HPT) [3]. As described in Chapter I, the OEIC and the OEID are distinguished by whether the incorporated devices form a circuit. According to this definition, the PPM is also classified into the OEID since optical signals are processed independently by each bistable switch and conducting elements are used only for power supply.

The PPM is proposed by the author based on the following considerations. The merits in production of Si IC's arise from the fact that the incorporated devices have the identical structure. To utilize the same merits in the integrated optoelectronics, identical optoelectronic devices should be integrated in large scale. The PPM has potential application to optical interconnections within computer systems and optical digital computing. They are essential parts in optical signal processings though the optical signal generation and detection described in Chapters III and IV are also important.

Conventional computers based on VLSI technologies suffer from communication problems such as interconnection bandwidth, clock skew, and von Neumann bottleneck [4-6]. These communication problems will be overcome by using optical signals for interconnections since light has inherent advantages of large bandwidth, dense parallel transmission, and non-interfering propagation [5,6]. To utilize optical signals in computers, optical computing based on purely optical phenomena has been proposed [7,8]. The "pure" optical computing has potentiality of ultra-high speed operation though it usually needs high optical power.

The required optical power can be reduced by using optoelectronic devices for signal processing. Although the speed of opto-

electronic devices is limited by electrons, the logic and memory functions can be obtained easily by the assistance of electronics. Large scale integration is indispensable for applying optoelectronic devices to computing. The PPM, a two-dimensional array of optoelectronic bistable switches, is just fitted for this requirement.

Besides the OEID consisting of an LED and a HPT, various kinds of optoelectronic bistable switches have been proposed [9-12], and the integration of more than one thousand devices has also been demonstrated [13]. Compared with them, the OEID in the PPM has advantages of inherent gain and unidirectionality for optical signals [14]. Furthermore, the OEID has flexibility in design since light emission and photodetection are done separately and the LED and the HPT can be used not only as an integrated device but as independent devices.

5-2. Integrated Device Structures

5-2-1. Operation principle

The optoelectronic bistable switch integrated in the PPM consists of an LED and an HPT. They are connected electrically in series and optical positive feedback from the LED to the HPT causes the bistability [3]. The switch takes "on" and "off" states and emits light in the on-state. The switch can be turned on by optical signal incident upon the HPT, while the bias voltage for the switch is decreased to turn off the switch. Therefore, the PPM including only the switches is written in and read out by optical signals, and erased by electrical signals. This type of PPM is named an electrically erased PPM (EE-PPM).

In some applications, however, an optically erasable PPM (OE-PPM), which can be written in and erased by optical signals, is desirable. To attain the function of optical erasing, an additional HPT for reset operation and a load resistor are also integrated in the unit cell of the OE-PPM. The switch and the reset HPT are wired in parallel and bias voltage is applied through a load resistor.

The equivalent circuit of the unit cell of the OE-PPM is shown

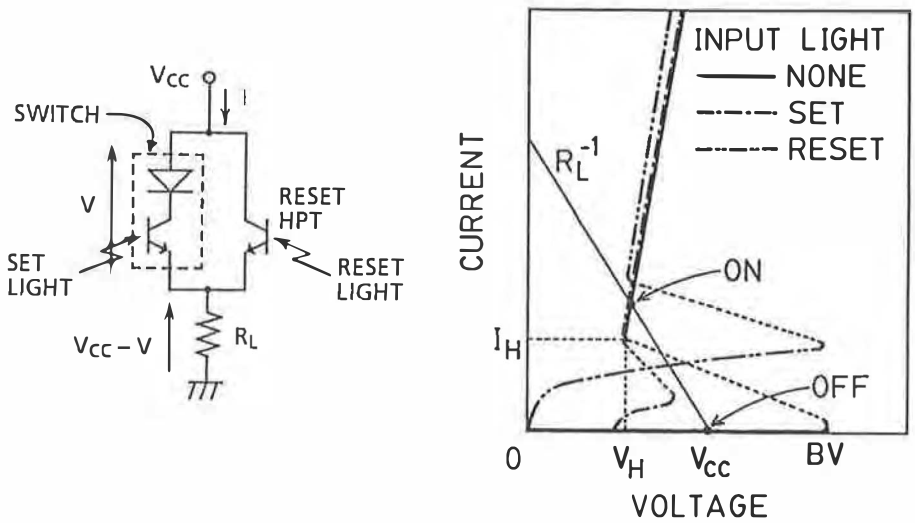


Fig. 5-1 Equivalent circuit and voltage - current characteristics of a unit cell integrated in the optically erasable photonic parallel memory (OE-PPM) to illustrate the operation principle of optical set and reset functions.

in Fig. 5-1 along with the voltage-current characteristics, by which the operation of the unit cell can be explained. Without input light, the thyristor-like characteristics shown by solid line is observed. This line and the load line determined by the bias voltage (V_{CC}) and the load resistor (R_L) have two intersections corresponding to the on-state and the off-state. When set light is incident upon the switch, the breakdown voltage is decreased and the intersection of the off-state disappears. Therefore, the switch in the off-state is turned on by the set light. In case that reset light is put into the reset HPT, the current through the reset HPT is added to the current through the switch. As a result, the intersection corresponding to the on-state vanishes and the switch in the on-state is turned off.

5-2-2. Electrically erased PPM

The structure of the EE-PPM is shown in Fig. 5-2 [1]. It contains 32 X 32 mesas isolated by etched grooves. The groove has a width of 4 μm and a depth of 5 μm, and the remained mesa has an area of 16 X 16 μm^2. Each mesa is the bistable switch consisting

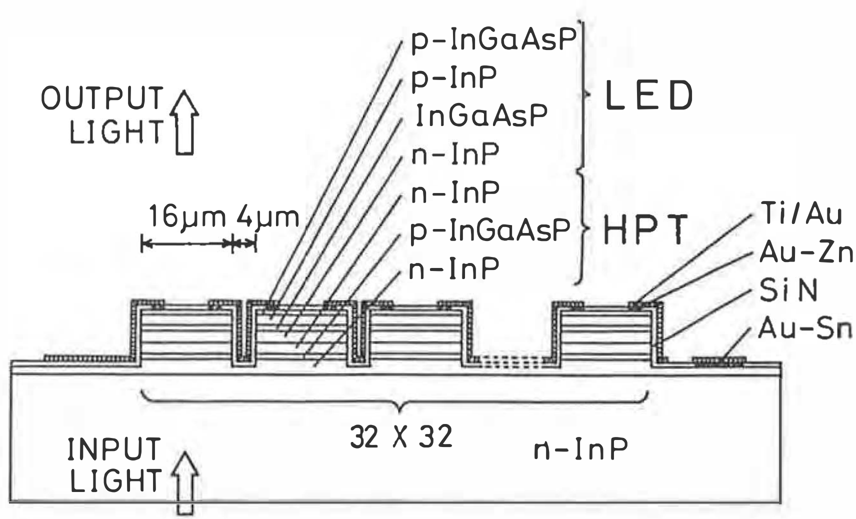


Fig. 5-2 Schematic cross-section of electrically erased photonic parallel memory (EE-PPM). Each mesa consisting of a light emitting diode (LED) and a heterojunction phototransistor (HPT) is an optoelectronic bistable switch.

of seven layers which are an n-InP emitter, a p-InGaAsP base, an n-InP collector, an n-InP clad, an InGaAsP active layer, a p-InP clad, and a p-InGaAsP cap. The first three and the rest four layers constitute HPT and LED, respectively. All the switches are wired in parallel with a Ti/Au interconnection metal. The Ti/Au plays also a role of optical isolation for the switches since it surrounds all the side walls of the mesas.

As shown in Fig. 5-2, input light is incident upon the HPT through the substrate and output light is emitted upward from the LED. This "passing-through" configuration can be attained by the fact that the substrate and the epitaxial layers other than the base of HPT and the active layer of LED are transparent for light with a wavelength of 1.3 μm which is used as input and output signals.

5-2-3. Optically erasable PPM

The structure of a unit cell integrated in the OE-PPM is shown in Fig. 5-3 [15]. It contains two mesas which corresponds to the switch and the reset HPT. The switch and the HPT mesas have areas

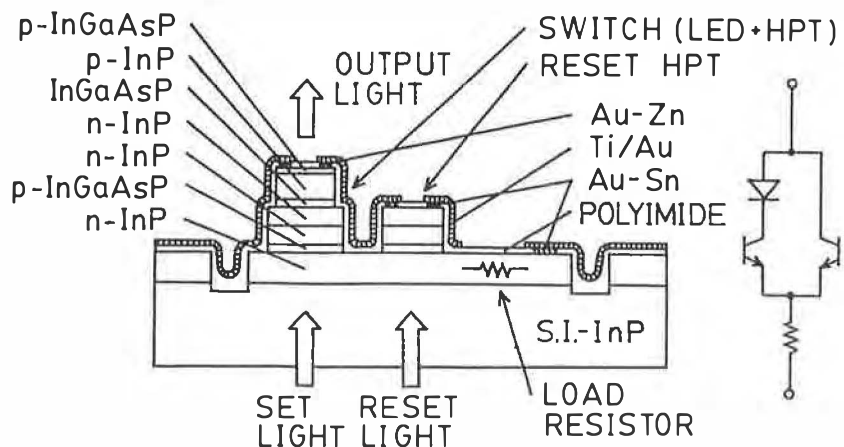


Fig. 5-3 Schematic cross-section of a unit cell integrated in the OE-PPM.

of $20 \times 20\ \mu m^2$ and $16 \times 16\ \mu m^2$, respectively, and the cell has an area of $60 \times 60\ \mu m^2$. The switch has just the same layer construction as the switch in EE-PPM, while the reset HPT consists of the lower four layers of the switch.

The substrate of the OE-PPM is a semi-insulating InP and the common emitter layer is used also as a load resistor. As shown in the equivalent circuit, the switch and the reset HPT are wired in parallel and bias voltage is applied through a load resistor. These electrical interconnections are attained in the array by connecting all the contacts on tops of both the switches and the reset HPT's with anode lines, and all the contacts on the load resistors with cathode lines.

5-3. Fabrication

To fabricate the EE-PPM, the seven layers are first grown on an n^+-InP substrate by LPE, which are an n-InP emitter ($1.5\ \mu m$, $5 \times 10^{17}\ cm^{-3}$), a p-InGaAsP base ($0.25\ \mu m$, $1 \times 10^{17}\ cm^{-3}$, bandgap wavelength $\lambda_g = 1.3\ \mu m$), an n-InP collector ($0.9\ \mu m$, $1 \times 10^{17}\ cm^{-3}$), an n-InP clad ($0.9\ \mu m$, $1 \times 10^{18}\ cm^{-3}$), an InGaAsP active layer ($0.3\ \mu m$, undoped, $\lambda_g = 1.3\ \mu m$), a p-InP clad ($1.0\ \mu m$, $5 \times 10^{17}\ cm^{-3}$), and a p-InGaAsP cap ($0.1\ \mu m$, $2 \times 10^{18}\ cm^{-3}$, $\lambda_g = 1.1\ \mu m$). Then the epitaxial layers are etched with reactive ion etching using a

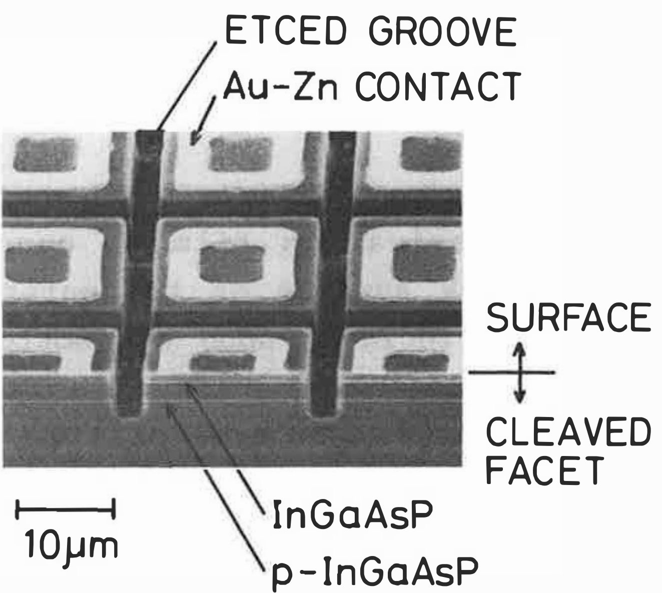


Fig. 5-4 SEM photograph of a cleaved mesas with ring anodes on a PPM chip. The grooves are etched with RIE using a mixture of Br_2 and Ar gases.

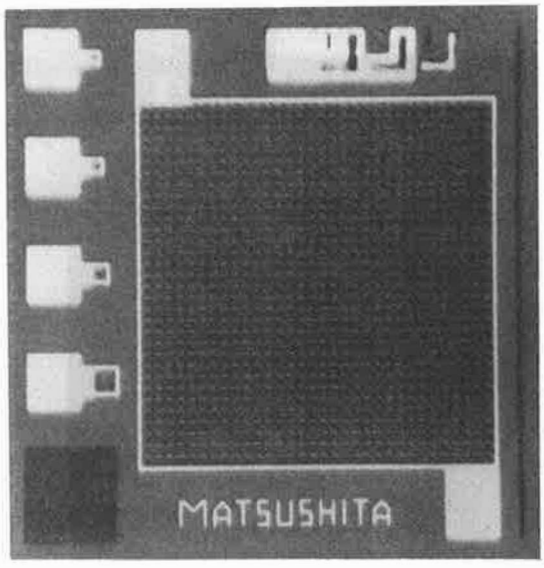


Fig. 5-5 Photomicrograph of a fabricated PPM chip. The chip has an area of $1.0 \times 1.0\ mm^2$ including bonding pads and single switches for testing. The area for the array is $640 \times 640 \mu m^2$.

mixture of Br_2 and Ar gases to form the grooves. After mesa formation, Au-Zn ring anodes are evaporated on the tops of the mesas and Au-Sn cathodes are outside of the mesas where the emitter is exposed. An SEM photograph of the cleaved mesas with the ring anodes is shown in Fig. 5-4.

After contact evaporation, a Ti/Au interconnection metal is evaporated on a SiN passivation film to connect all of the anodes. Finally, the back surface of the wafer is polished so that input light can be incident upon the bottom of the switch without scattering. The photomicrograph of a fabricated chip is shown in Fig. 5-5. The chip has an area of $1.0 \times 1.0\ mm^2$ including bonding pads and single switches for testing, while the active area for the array is $640 \times 640\ \mu m^2$.

The fabrication steps of the OE-PPM is basically the same as those of the EE-PPM except for the following three points. First, the substrate is semi-insulating InP to form the load resistors. Second, the switch and the HPT mesas are formed with wet chemical etching to utilize preferential etchants. Thirdly, passivation

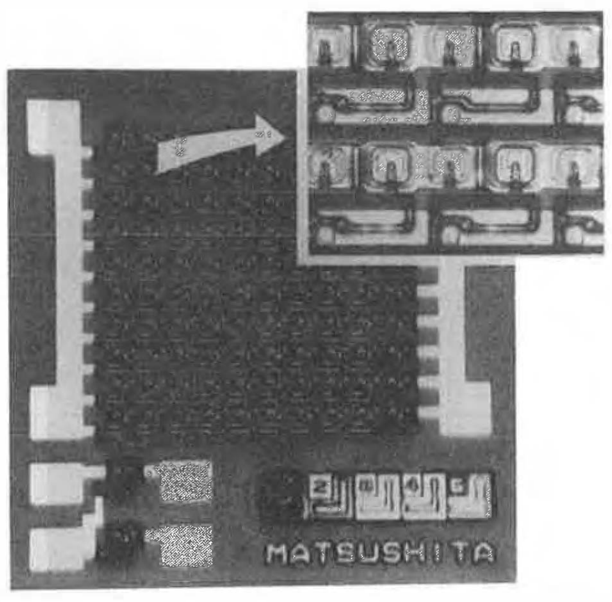


Fig. 5-6 Photomicrograph of a fabricated OE-PPM chip including 10 X 10 cells. The chip has an area of $1.0 \times 1.0\ mm^2$, and the area for the array is $600 \times 600\ \mu m^2$. Inset shows the magnified photograph of four cells.

film is changed from SiN_x to polyimide to obtain the semi-planar surface for the metallization of the anode and the cathode lines. The photomicrograph of a fabricated chip including 10 X 10 array is shown in Fig. 5-6. The chip size is 1.0 X 1.0 mm^2.

5-4. Characteristics of EE-PPM's

5-4-1. Array operation

The experimental setup for operating the EE-PPM is shown in Fig. 5-7 together with the schematic diagram of memory operation. To operate the EE-PPM, bias voltage ranging from 1.6 V to 2.2 V is first supplied to all the switches without input light. They are in the off-state and no light emission is observed. Then the light emitted from a 1.3 μm laser diode is incident upon the bottom of the chip through a single mode fiber with a focusing lens. Since a photomask is set between the lens and the chip, the light is incident only upon limited number of switches. The selected switches are turned on and emit output light. The output

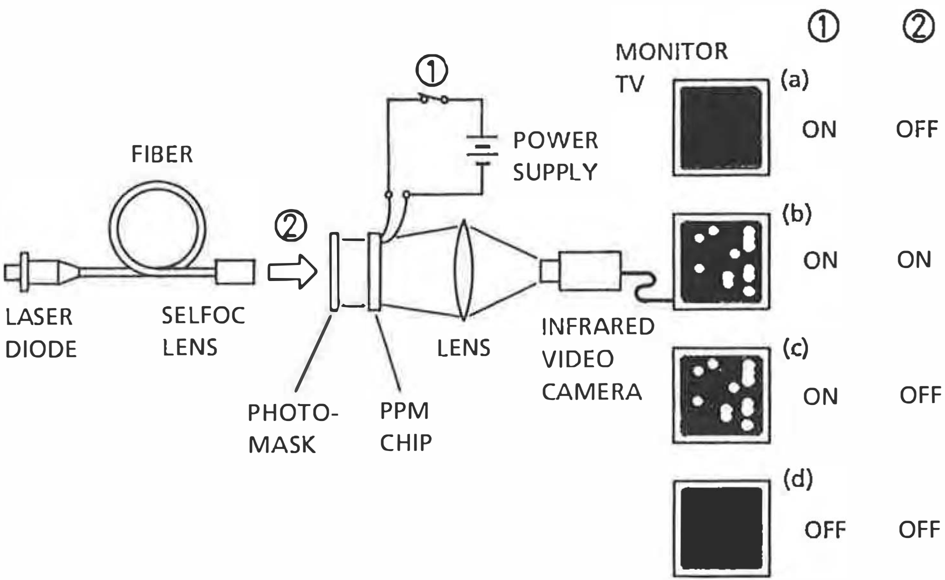


Fig. 5-7 Experimental setup for operating the EE-PPM together with the schematic diagram of memory operation: (a) initial state, (b) write-in operation, (c) memory and read-out operation, and (d) reset operation.

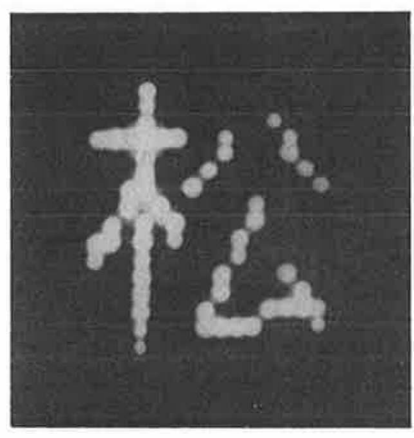
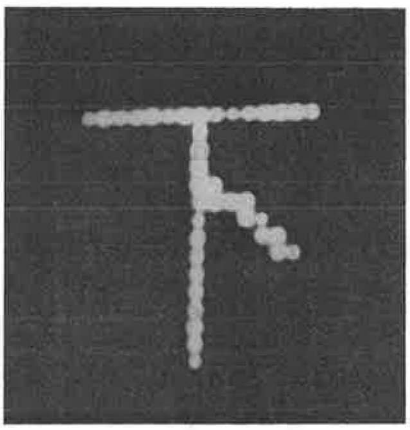



Fig. 5-8 Infrared video camera image of an EE-PPM chip in memory operation. A Chinese characters meaning "Matsu-Shita" are memorized and read out.

light is observed through an infrared video camera focused on the top of the chip. The on-state is maintained after removing the input light and the selected switches keep on emitting light. All the switches are turned off by making the bias voltage zero. Infrared images of the EE-PPM chip in memory operation are shown in Fig. 5-8. Chinese characters meaning "Matsu-Shita" are displayed.

5-4-2. Static characteristics

Typical voltage - current characteristics of a single switch integrated in the EE-PPM are shown in Fig. 5-9. As shown in Fig. 5-9(a), a thyristor-like voltage-current curve is observed unless input light is incident. In this curve "on-state" and "off-state" are clearly distinguished. As input optical power is increased, the breakdown voltage is decreased and a diode-like curve shown in Fig. 5-9(b) is observed when the input power measured at the fiber end is 175 μW. In case of operating it with a constant bias voltage, the switch is turned on before this condition. In other words, the input optical power necessary to turn on the switch (set power) depends on the bias voltage and the maximum value is equal to the input optical power necessary to obtain the diode-like curve.

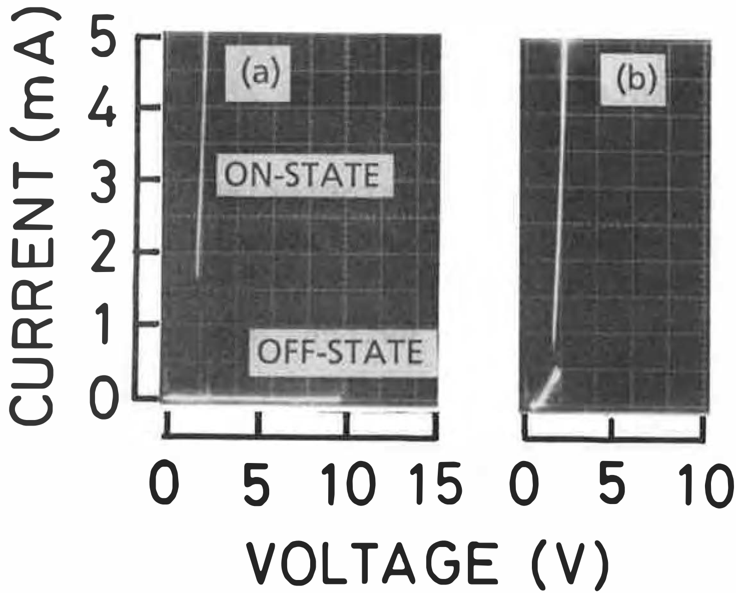


Fig. 5-9 Voltage - current characteristics of a single switch with an InP collector and a thick (∿0.25 μm) base: (a) without input light and (b) with an input light of 175 μW.

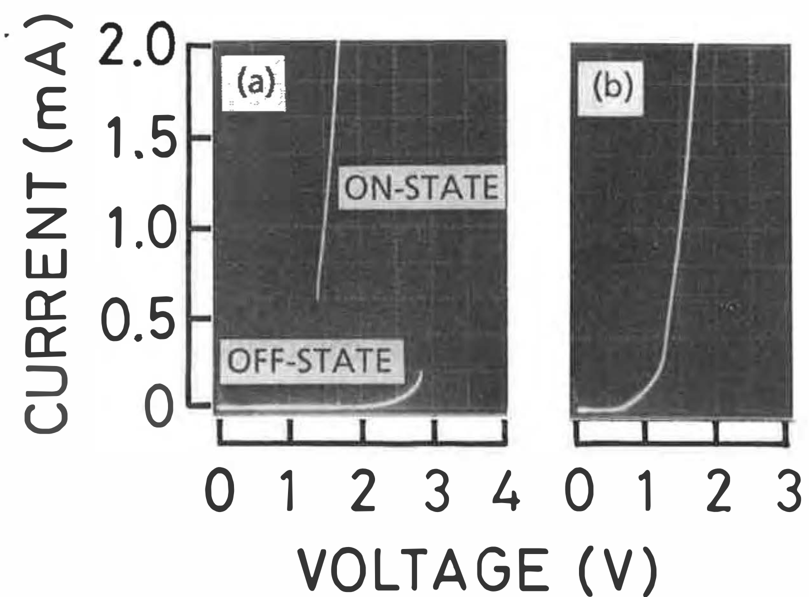


Fig. 5-10 Voltage - current characteristics of a single switch with a quarternary collector and a thin (∿0.15 μm) base: (a) without input light and (b) with input light of 20 μW.

For the operation of PPM, it is desirable to decrease both the set power and the dissipation current in the on-state. The minimum current to maintain the on-state (holding current) can be found from voltage - current characteristics and is 1.6 mA for the switch shown in Fig. 5-9. The characteristics for another switch with a holding current of 600 μA are shown in Fig. 5-10. The input optical power necessary to obtain diode-like curve has also been reduced to be 20 μW. For this switch, the collector of HPT has been changed to InGaAsP and the base has been made to be thinner (∿ 0.15 μm). As can be seen in Fig. 5-10(a), the breakdown voltage without input light is also reduced since breakdown caused by the optical positive feedback occurs at lower bias voltage for the switch with a thinner base.

To separate the cause for the reduction of holding current, the relations between breakdown voltage without input light and holding current have been measured for three types of switches

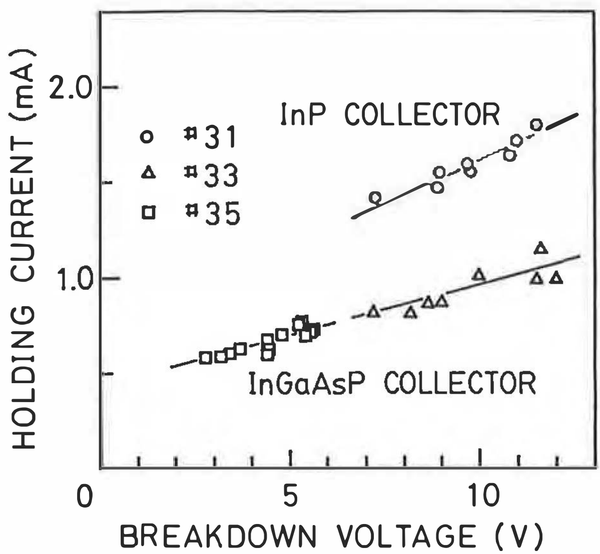


Fig. 5-11 Relations between breakdown voltage without input light and holding current. The switches are selected from three different wafers: with an InP collector and a thick base (#31), with a quarternary collector and a thick base (#33), and with a quarternary collector and a thin base (#35).

which are selected from three different wafers. They are the wafer with an InP collector and a thick (∿0.25 μm) base (#31), with a quarternary collector and a thick base (#33), and with a quarternary collector and a thin (∿0.15 μm) base (#35).

The results are shown in Fig. 5-11. The breakdown voltage depends on the thickness of the base layer and the various values of breakdown voltage observed in switches on the same wafer is attributed to non-uniformity of layer thickness. The switches with a quarternary collector have smaller holding current than those with an InP collector, and the switches with lower breakdown voltage, which corresponds to thinner base, have smaller holding current. The mechanism which determines holding current is discussed in Section 5-7-1.

5-4-3. Switching speed

To evaluate the operation speed of PPM, turn-on and turn-off speed have been measured as follows. As for turn-on speed, light pulses with various pulse widths are incident upon the switch and set power is measured. The results are shown in Fig. 5-12. The

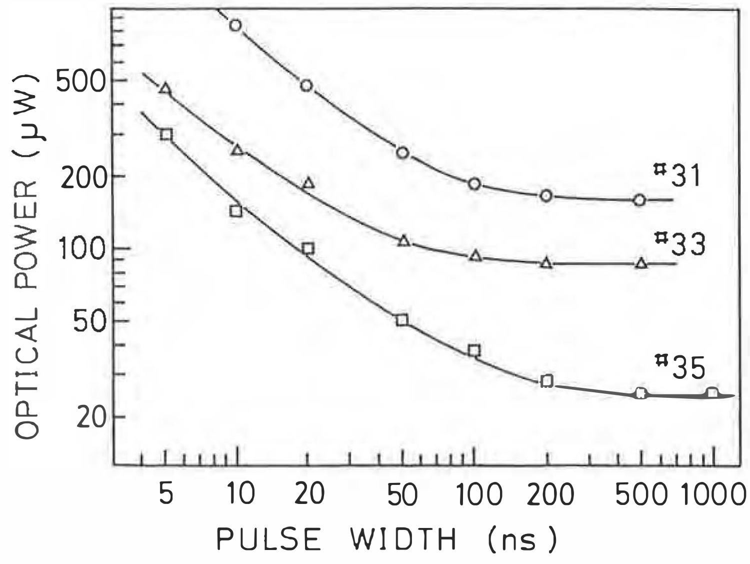


Fig. 5-12 Relations between pulse width of input light and set power necessary to turn on the switch for single switches integrated in PPM chips on wafers #31, #33, and #35.

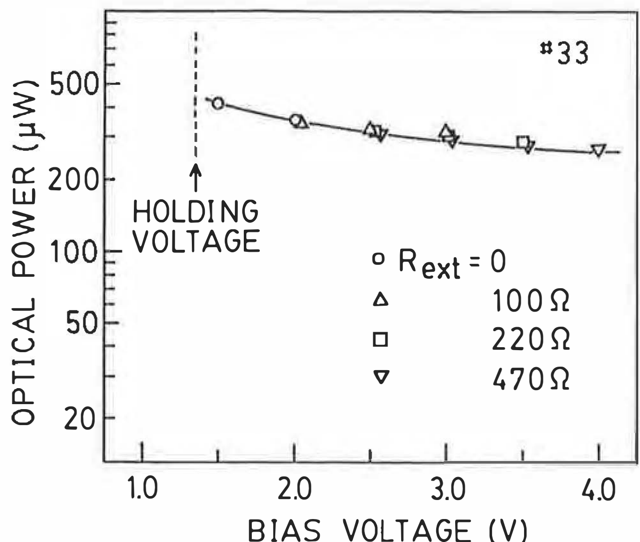


Fig. 5-13 Relation of bias voltage and set power for input light pulse with a width of 10 ns. External load resistors (R_{ext}) are connected between the switch and the power supply in the measurements for high bias voltages.

measurement has been done for three types of PPM chips on wafers #31, #33, and #35 described in the previous section. The light pulse with a width of 5 ns can turn on the switches on wafers #33 and #35 though the set power is increased as the pulse width is decreased. The product of set power and pulse width for short pulse region is calculated to be 1.5 pJ for the switch on #35.

The results shown in Fig. 5-12 are obtained using a bias voltage of 1.9 V. The set power slightly depends on the bias voltage whether the pulse width is short or long. The dependence of set power on bias voltage is shown in Fig. 5-13. It has been measured for #33 at the pulse width of 10 ns. The holding voltage in the figure means the minimum voltage necessary to maintain the on-state. An external load resistor (R_{ext}) was used in measurement for high bias voltage to prevent the switch from flowing excessive current in the on-state. This load resistor also does not affect the switching speed.

To measure the turn-off speed, the switches are first turned on and then the bias voltage is made to be zero during a short

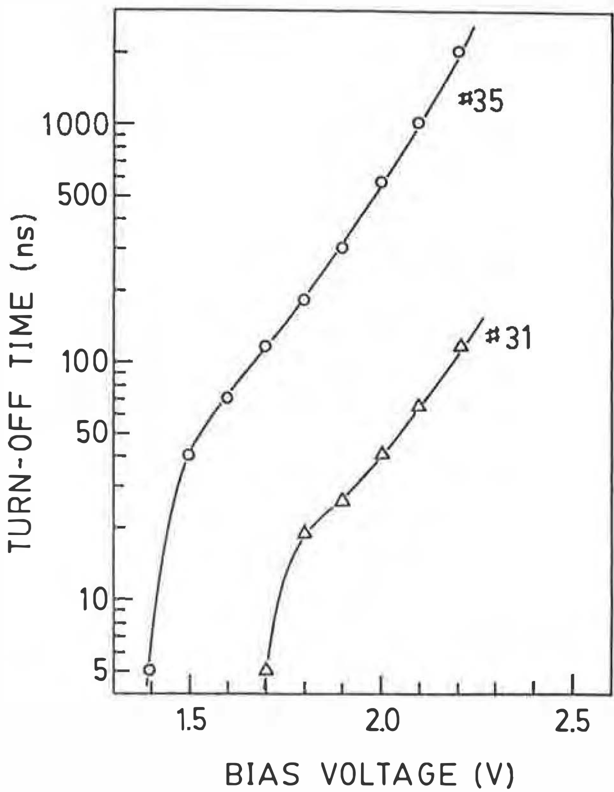


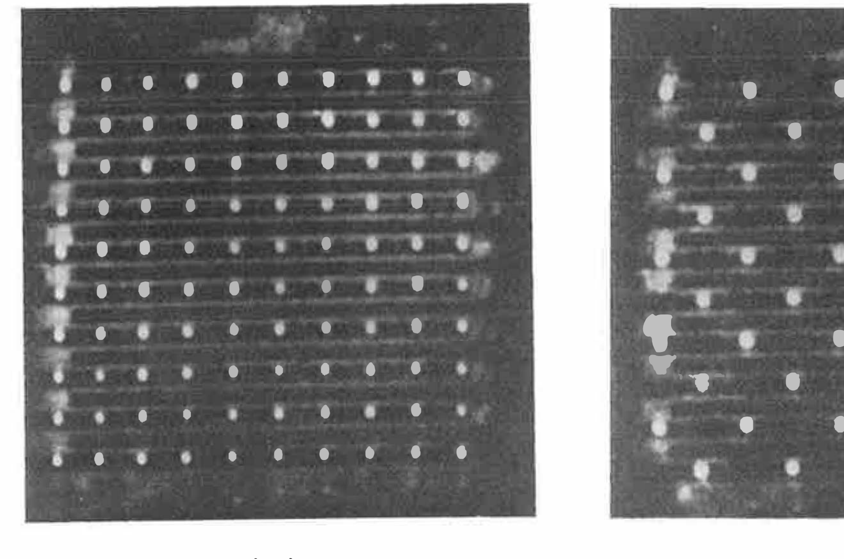
Fig. 5-14 Relations between bias voltage in the on-state and the length of period necessary to turn off the switch (turn-off time).

period. The length of period necessary to turn off the switches has been measured for wafers #31 and #35 in relation to the bias voltage in the on-state. The results are shown in Fig. 5-14. The turn-off time strongly depends on the bias voltage and the value less than 5 ns is obtained in case of setting the bias voltage close to the holding voltage. To keep the on-state stably, however, some margin is necessary between the bias voltage and the holding voltage. Therefore, the reasonable value for turn-off time is thought to be 20 - 40 ns.

5-5. Characteristics of OE-PPM's

5-5-1. Array operation

The set operation of the OE-PPM is just the same as that of the EE-PPM. The set light is incident upon selected switches,



(a) (b)

Fig. 5-15 Infrared image of an OE-PPM chip in memory operation: (a) all of 100 switches turned on and emitting light, and (b) half of the switches turned off by optical signals and the rest switches emitting light.

which are turned on and emit output light. To turn off the switch, the reset light is put into the reset HPT. Differently from that of the EE-PPM, this reset operation is selective, that is, only the selected switches are turned off by the reset light. Infrared images of the OE-PPM chip in memory operation are shown in Fig. 5-15. All of 100 switches are turned on by the set light in Fig. 5-15(a), and half of the switches are turned off by the reset light in Fig. 5-15(b).

5-5-2. Static Characteristics

Typical voltage - current characteristics of a switch in the OE-PPM without illumination are shown in Fig. 5-16. This switch has a holding current of 130 μA. The drastic reduction of holding current has been attained though the switch has just the same layer structure as #31 of the EE-PPM. The reason of the reduction in dissipation current is related to the fabrication process which is discussed in Section 5-7-1.

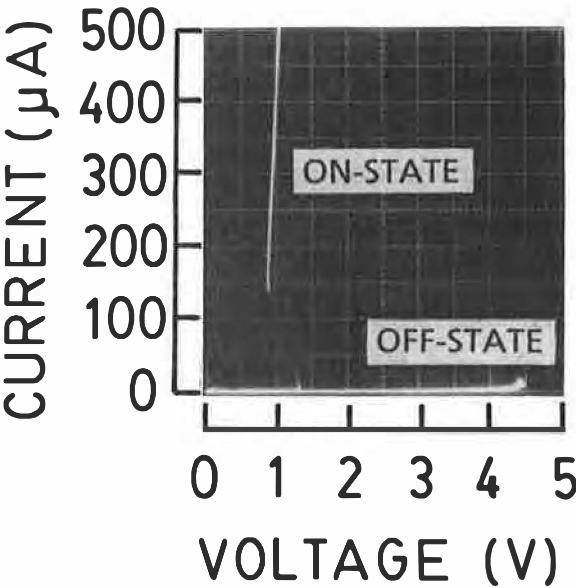


Fig. 5-16 Voltage - current characteristics of a single switch integrated in the OE-PPM. The holding current is reduced to 130 μA.

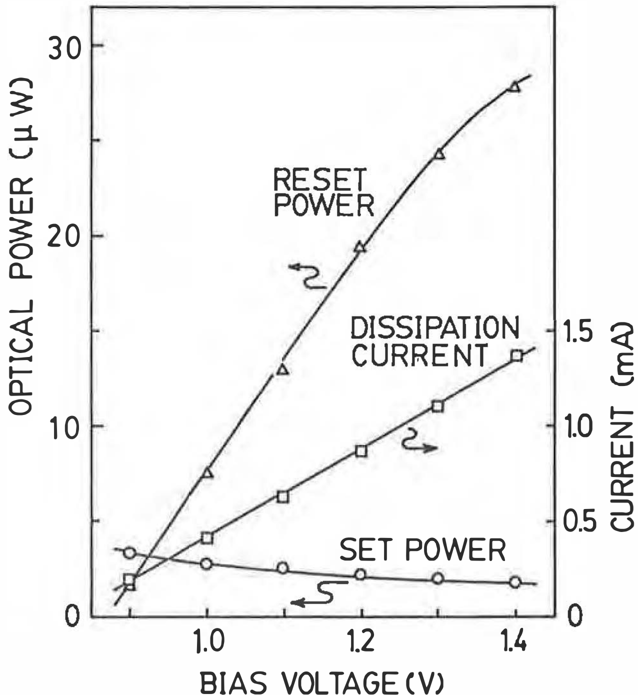


Fig. 5-17 Optical power necessary to set or reset a switch in the OE-PPM in relation to bias voltage along with the dissipation current of the switch in the on-state.

The optical power to set or reset the switch (set or reset power) has been measured for the OE-PPM in relation to the bias voltage. The results are shown in Fig. 5-17 along with the dissipation current of the switch in the on-state. As can be seen from Fig. 5-17, the set power does not strongly depend on the bias voltage. This tendency is just the same as the EE-PPM though the set power is much smaller than the EE-PPM.

On the other hand, the reset power increases as the bias voltage is increased which can be expected from the operation principle. The reset power is thought to reach zero when the bias voltage is reduced to the holding voltage. To keep the on-state stably, however, some margin for the bias voltage is necessary. The measured minimum reset power is 1.6 μW at a bias voltage of 0.9 V which is enough voltage for stable operation. The set power and the dissipation current at the same bias condition are 3.4 μW and 200 μA, respectively.

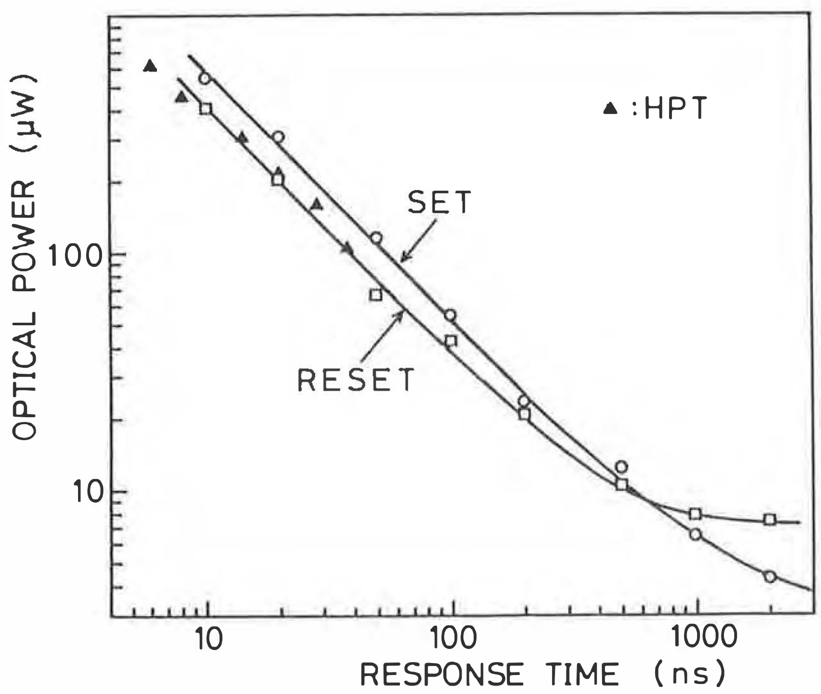


Fig. 5-18 Relations between pulse width of input light and set or reset power of a switch in the OE-PPM. The response time of the HPT is also plotted.

5-5-3. Switching speed

To evaluate the operation speed of OE-PPM, short light pulse is used as a set and a reset signal, and the set and the reset power have been measured. The results obtained at a bias voltage of 1.0 V are shown in Fig. 5-18. The light pulse with a width of 10 ns can set or reset the switch though the set and reset power are increased to 547 μW and 406 μW, respectively. The switching energy of about 5 pJ coincides with that of #31 of the EE-PPM.

5-6. Proposals for Application of the PPM

In this section, applications of the PPM are described. Though they are just the proposals now, it can be expected that they will be realized in the near feature.

5-6-1. Crossbar switchboard

When the bias voltage of the PPM is modulated between the holding voltage and the breakdown voltage, modulated optical signals are emitted from the switches in the on-state, while the switches in the off-state do not emit light. Combining this function with optical set or reset of the switches, a crossbar switchboard can be realized as shown in Fig. 5-19.

The switchboard consists of three layers and the middle layer is the OE-PPM. The anodes of the switches in the OE-PPM are wired along each row and electrical modulation signal is supplied to each row. The modulated optical signals emitted from the switches are incident upon the photodetectors on the top layer. The photodetectors arranged in column direction are wired and the optical signals detected by the photodetectors along each column are converted to an electrical signal.

As a result, the crossbar switching of electrical signals from row to column is attained by turning on the switches at the crossings where connections should be made. The bottom layer is an array of light sources, such as matrix addressable surface emitting laser array (MASELA) [16], which changes the points of connections by turning on or off the switches selectively.

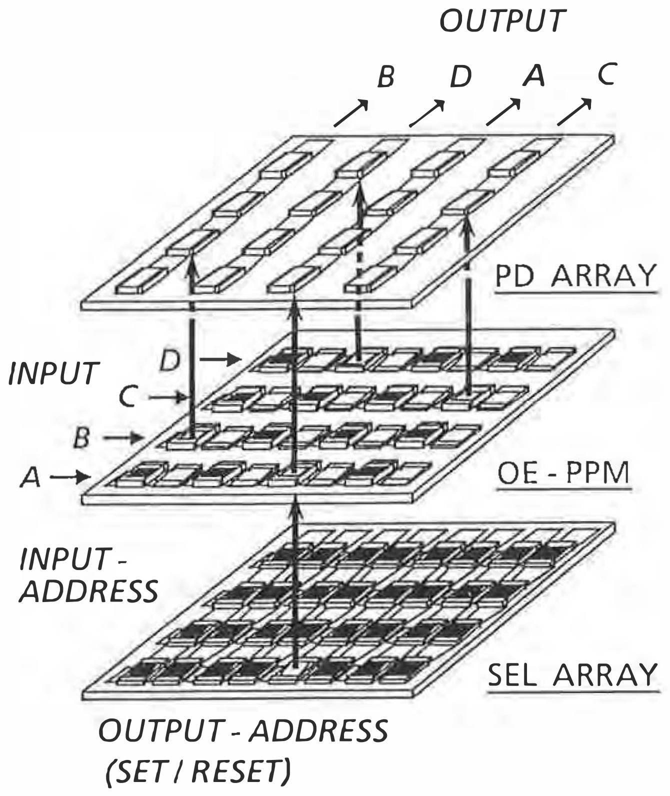


Fig. 5-19 Optical crossbar switchboard consisting of an OE-PPM, a photodetector (PD) array, and a surface emitting laser (SEL) array.

5-6-2. Free-space interchip connections

Another example of optical interconnections based on the PPM is shown in Fig. 5-20. This is a free-space reconfigurable interchip connection. Each chip has an optical transmitter and a photodetector. The optical transmitter has the same construction as the crossbar switchboard shown in Fig. 5-19 except that the top layer is not a photodetector array but a holographic optical element (HOE), and all the switches in OE-PPM are wired in parallel.

In this application, it is desirable to change LED's in the OE-PPM to vertical cavity surface emitting lasers. The laser beam from the OE-PPM is diffracted by the HOE which changes the emission angle of the beam corresponding to the position of incident beam. The diffracted beam is reflected by mirror and detected by

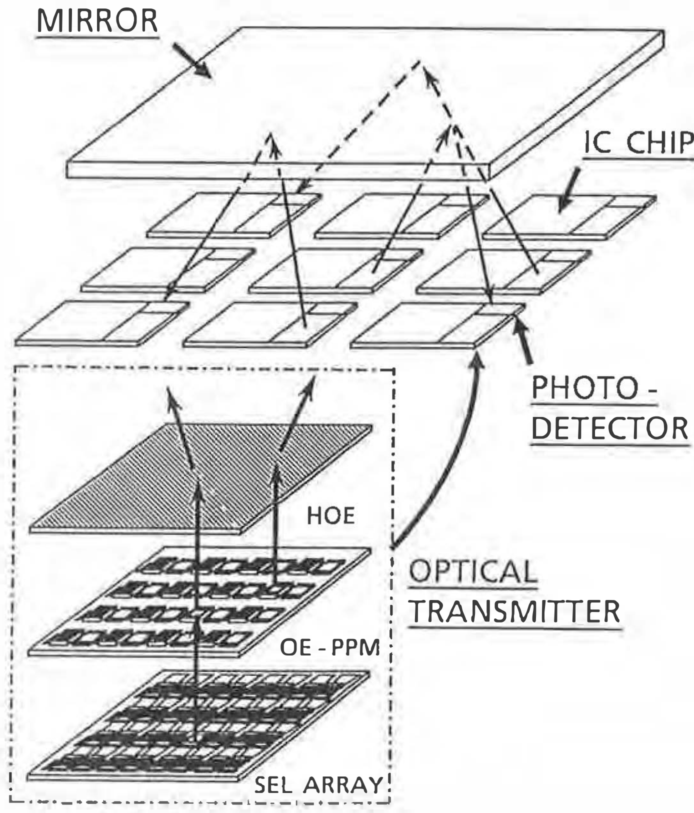


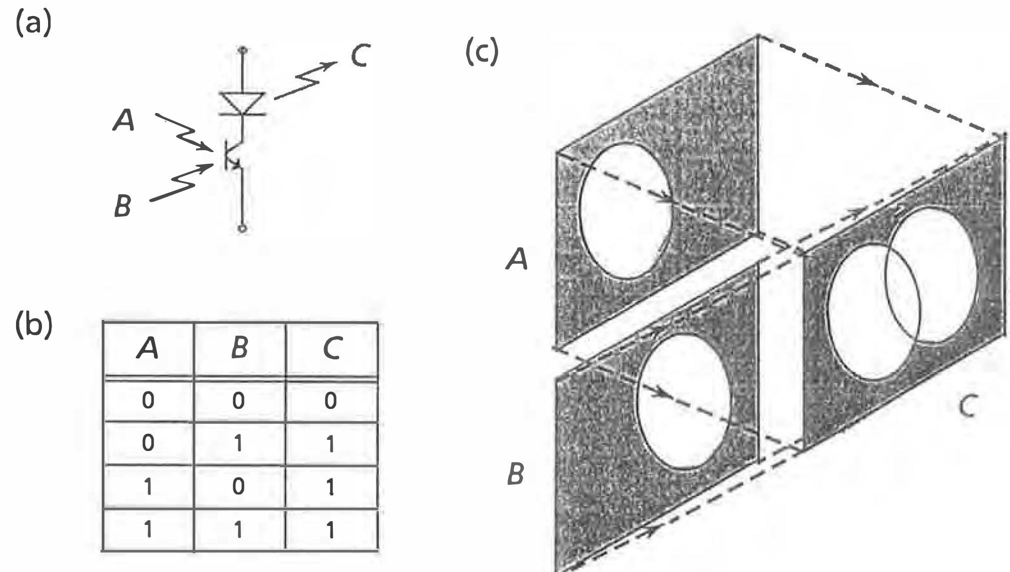
Fig. 5-20 Free-space reconfigurable interchip connections using optical transmitters consisting of an OE-PPM, a SEL array, and a holographic optical element (HOE).

the photodetector on another chip. Therefore, the address of the chip, to which the optical signal is sent, can be chosen by turning on the switch in the OE-PPM selectively.

Though this configuration can be attained only with the MASELA and the HOE, electrical modulation signals and address signals can be separated and one-to-many routes as well as one-to-one can be constructed by adding the OE-PPM.

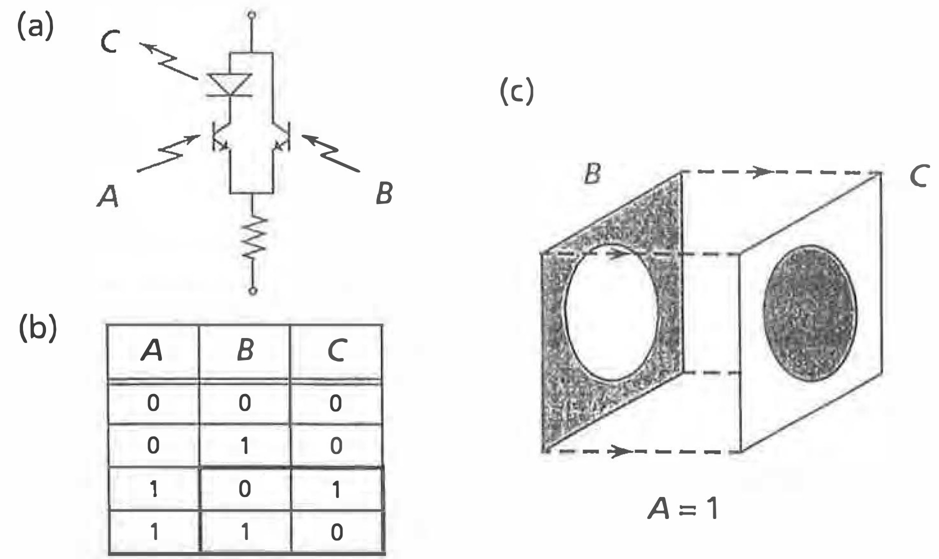
5-6-3. Optical parallel logic gates

The optoelectronic bistable switch can be operated as an OR gate, because an output signal corresponding to A OR B is emitted when input signals of A and B are incident upon the switch either sequentially or simultaneously. Therefore, the EE-PPM can be operated as a 1 Kbit parallel OR gate as shown in Fig. 5-21.



A	B	C
0	0	0
0	1	1
1	0	1
1	1	1

Fig. 5-21 Optical parallel OR gate based on the EE-PPM: (a) input and output configuration, (b) truth table, and (c) illustration of array operation.



A	B	C
0	0	0
0	1	0
1	0	1
1	1	0

Fig. 5-22 Optical parallel NOT gate based on the OE-PPM: (a) input and output configuration, (b) truth table, and (c) illustration of array operation.

Furthermore, the OE-PPM has a function of a parallel NOT gate shown in Fig. 5-22. When an input signal A is incident upon the switch and B upon the reset HPT, the output is to be $A \cdot \overline{B}$. If A is set to be 1, the output becomes $\overline{B}$. Since both OR and NOT functions are available, all the logic functions can be attained in parallel by logic gates using the PPM's.

5-7. Discussion

5-7-1. Analysis for dissipation current

The dissipation current (I_d), the output optical power (P_{out}), and the input optical power (P_{in}) of the switch are related by

$$P_{out} = \eta_{ext} I_d \tag{5-1}$$

$$I_d = G_{opt} (k P_{out} + P_{in}), \tag{5-2}$$

where η_{ext} is the external efficiency of the LED in W/A, G_{opt} is the optical gain of the HPT in A/W, and k is the ratio of the feedback optical power to the output optical power. In general, η_{ext} and G_{opt} is decreased as I_d decreases, while k is considered to be approximately constant and equal to unity ideally since downward light emitted from the LED has the same power as upward light.

In case of $P_{in} = 0$, the trivial solution of Eqs. (5-1) and (5-2) is $I_d = 0$, which denotes the off-state. The other solution corresponding to the on-state is $k \eta_{ext} G_{opt} = 1$. Therefore, it is important to fabricate an LED with high efficiency and an HPT with high gain in low current region to obtain the switch with low dissipation current. As can be seen from Eq. (5-2), such a switch can also reduce the set power.

The above discussion can qualitatively explain the experimental results shown in Fig. 5-11. The optical gain of the HPT is the product of optical absorption efficiency (η_a) and current gain (β). The switches with a quarternary collector have smaller holding current than those with an InP collector because the quarternary collector increases η_a. The switches with a thinner

base have smaller holding current since it increases β.

The reason why the switches in the OE-PPM have smaller holding current than the switches in the EE-PPM is also explained as follows. The gain of HPT and the efficiency of LED in low current region are related to the surface recombination and affected by surface defects on the side walls of the switch mesa. The mesa of the EE-PPM, which is formed by dry etching and covered by plasma-deposited SiN_x, suffers severe damage which increases the surface defects, while the mesa of the OE-PPM is damaged only slightly since it is formed by wet etching and covered by polyimide.

5-7-2. Relation of input and output power

The typical optical gain of an HPT (G_{opt}) included in the switch has been measured to be 116 A/W at a bias voltage of 1.5 V. The internal efficiency of an LED (η_{int}) is 0.11 W/A, which is the conversion efficiency from the injected current to the optical power fedback from the LED to the HPT. Since $\eta_{int} = k\,\eta_{ext}$, the product of $\eta_{int}\,G_{opt}$ is always unity in the on-state as described in the previous section. To satisfy this condition, the bias voltage of the HPT in the on-state is decreased and the optical gain of the HPT becomes smaller. Therefore, the ratio of the feedback power to the set power is always greater than unity.

However, the ratio of the output power to the set power is smaller than this value since the output light from the LED is shaded by the contact and interconnection metals. The external efficiency of the LED is approximately 0.01 W/A. In case of the switch shown in Fig. 5-17, the output power at a bias voltage of 0.9 V is about 2 μW, which is smaller than the set power. However, the ratio of the output power to the set power becomes greater than unity as increasing the bias voltage.

5-7-3. Improvement for switching speed

Based on the discussion in Section 5-7-1, the set power as well as the holding current is reduced by using a quarternary collector or a thin base as demonstrated in Fig. 5-12, where the

set power for long pulse region coincides with that in DC mode operation. However, the set power for the switch with a thin base (#35) approaches to that for the switch with a thick base (#33) in short pulse region. The set power is also reduced by decreasing the surface defects as shown for the OE-PPM in Fig. 5-18 though the set power in short pulse region is not improved.

To find the limitation factor of the switching speed, the response delay time of the HPT has been measured. It is also shown in Fig. 5-18. The set and reset speed coincides with the response time of the HPT which is mainly limited by the charging time of the emitter - base and the collector - base capacitances with photocurrent. Therefore, the response time of the switch is not improved by using a thin base or decreasing the surface defects. It will be improved by reducing the capacitances of the HPT which is simply attained by shrinking the device size.

5-8. Summary

A photonic parallel memory (PPM), an array of optoelectronic bistable switches, has been proposed and fabricated. The switch consists of a heterojunction phototransistor (HPT) and a light-emitting diode (LED), and optical positive feedback from the LED to the HPT is the cause of bistability. In addition to the electrically erased (EE) PPM having only switches, an optically erasable (OE) PPM has also been demonstrated. The optical reset function is attained by an additional HPT connected to the switch electrically in parallel.

The memory operation of the PPM with functions of optical write-in, read-out, and erasing has been demonstrated. The optical crossbar switchboard, the free-space reconfigurable interchip connections, and the parallel logic gates have been proposed based on the PPM. The factors determining the holding current, the optical gain, and the switching speed have been analyzed and clarified.

The important quantitative results obtained in this chapter are as follows:

1) The integration scales attained for the EE-PPM and for the OE-PPM are 1 Kbit (32 X 32) and 100 (10 X 10), respectively. Both of them have a chip size of 1.0 X 1.0 mm^2.
2) The holding current and the set power are 1.6 mA and 175 μW for the switch in the EE-PPM with an InP collector and a thick (0.25 μm) base. They have been improved to 600 μA and 20 μW by using a quarternary collector and a thin (0.15 μm) base.
3) The light pulse with a width of 5 ns can turn on the switch in the EE-PPM, and the switching energy in the short pulse region is 1.5 pJ.
4) The switch in the OE-PPM has a holding current of 130 μA, a set power of 3.4 μW, and a reset power of 1.6 μW. Compared with the EE-PPM, the holding current and the set power are improved since the damage for the side walls of switch mesas are reduced by using wet etching and polyimide passivation.

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VI. CONCLUSIONS

The integrated optoelectronics based on InGaAsP/InP have been studied for application to optical signal processings. Both the fabrication of integrated structures and the characterization of fabricated devices are concerned in the study. The InGaAsP/InP materials system is very important for application to long-wavelength optical fiber communications. The process technologies for InGaAsP/InP have been upgraded and the three devices for optical signal processings have been developed.

In Chapter II, the process technologies for the InGaAsP/InP materials system are described. The process conditions have been examined for epitaxial growth, insulator film deposition, etching, dopant diffusion, and metallization. Especially for the etching and the metallization, new technologies, i.e., the reactive ion etching (RIE) with Br_2-containing gases and the transmission line model (TLM) method with a new contact arrangement have been proposed. The reliable technologies have been developed for all the processes, and they are applied to device fabrications described in the following chapters.

In Chapter III, the integration of a laser diode and a passive waveguide is described. Two new integrated structures, a self-aligned integrate loaded (SAIL) guide and a passive/active loaded (PAL) guide, have been proposed. Three structures including these two and a bundle-integrated-guide (BIG) have been fabricated. The guiding loss of the waveguide and the coupling efficiency between the laser and the waveguide are evaluated for these three structures. The SAIL guide is also applied to the integrated passive cavity (IPC) laser consisting of an active cavity and a long passive cavity. It exhibits stable single longitudinal mode oscillation with a narrow spectral linewidth.

In Chapter IV, the integration of a pin photodiode and an amplifier circuit is described. The monolithic photoreceiver incorporating a pin photodiode (PD), four junction field effect transistors (FET's), four level shift diodes, and a feedback resistor has been designed and fabricated successfully. Both the static and the high-frequency characteristics show that the pho-

toreceiver operates normally with a single 5 V power supply. The bandwidth has been measured with respect to the dissipation current for three types of photoreceivers which are distinguished by the gate length and the feedback resistance. The experimental results are well explained by theoretical considerations and coincide with the results of computer circuit simulation. Transmission characteristics have been measured to evaluate the sensitivity. It is limited by the 1/f noise of the front-end FET and has been improved by increasing the feedback resistance.

In Chapter V, a photonic parallel memory (PPM), which is an array of optoelectronic bistable switches, has been proposed and fabricated. The switch consists of a heterojunction phototransistor (HPT) and a light-emitting diode (LED), and optical positive feedback from the LED to the HPT is the cause of bistability. In addition to the electrically erased (EE) PPM being an array of the switches, an optically erasable (OE) PPM has also been demonstrated. The optical reset function is attained by an additional HPT connected to the switch electrically in parallel. The memory operation of the PPM with functions of optical write-in, readout, and erasing has been demonstrated.

The major and important results obtained through this study are as follows:

1) The process technologies for the InGaAsP/InP materials system, such as epitaxial growth, insulator film deposition, etching, dopant diffusion, and metallization, have been developed.
2) By using the reactive ion etching (RIE) with a mixture of Br_2 and Ar gases, smooth vertical walls have been obtained for InGaAsP/InP crystals with a high etching rate of about 2 μm/min.
3) Based on a new transmission line model (TLM) method, the contact resistivities of ohmic contacts on InGaAsP/InP have been evaluated.
4) Two types of new integrated structures comprising a laser diode and a passive waveguide, i.e., a self-aligned integrated loaded (SAIL) guide and a passive/active loaded (PAL)

guide have been proposed, and three types of integrated passive cavity (IPC) lasers including these two and a bundle-integrated-guide (BIG) have been fabricated.

5) A SAIL guide IPC laser with a 3.55 mm-long passive cavity has been successfully fabricated and operated with a rather low threshold current of 58 mA.
6) The threshold currents of the SAIL, the PAL, and the BIG-IPC lasers have been measured with respect to the passive cavity length, from which the coupling efficiency and the guiding loss are evaluated.
7) The long IPC laser exhibited stable single longitudinal mode oscillation with the maximum side-mode suppression ratio of more than 30 dB.
8) The spectral linewidth of the IPC laser has been measured by utilizing a delayed self-heterodyne technique. The linewidths of 1 - 2 MHz are easily obtained and the minimum value is about 900 kHz at the output power of 6 mW.
9) Monolithic photoreceivers incorporating a pin photodiode, four junction FET's, four level shift diodes, and a feedback resistor have been designed and fabricated.
10) The output resistance of the FET is drastically reduced in the frequency range from 10 Hz to 1 kHz and becomes constant above 100 kHz. This phenomenon is thought to be caused by the slow traps located at the interface between the Fe-doped InP substrate and the FET channel.
11) The highest 3 dB bandwidth of 285 MHz has been obtained for the photoreceiver with a gate length of 3 μm and a feedback resistance of 1.2 kΩ.
12) The minimum optical power to obtain a bit error rate of 10^{-9} at the bit rate of 120 Mbit/s is -27.1 dBm for the photoreceiver with a feedback resistance of 1.2 kΩ and -31.2 dBm for that of 3.6 kΩ.
13) The maximum bandwidth of the photoreceiver with self-aligned gate FET's is 360 MHz. The computer circuit simulation shows that it will be improved to 900 MHz if the pinch-off voltage of the FET's is precisely controlled.

14) A 1 Kbit electrically erased photonic parallel memory (EE-PPM) and a 100 bit optically erasable photonic parallel memory (OE-PPM) have been successfully fabricated.
15) The holding current and the set power are 1.6 mA and 175 μW for the switch in the EE-PPM with an InP collector and a thick (0.25 μm) base. They have been improved to 600 μA and 20 μW by using a quarternary collector and a thin (0.15 μm) base.
16) The optical pulse with a width of 5 ns can turn on the switch in the EE-PPM, and the switching energy in the short pulse region is 1.5 pJ.
17) The switch in the OE-PPM has a holding current of 130 μA, a set power of 3.4 μW, and a reset power of 1.6 μW. Compared with the EE-PPM, the holding current and the set power are improved since the damage for the side walls of switch mesas is reduced by using wet etching and polyimide passivation.
18) The mechanisms determining holding current, optical gain, and switching speed have been analyzed, and the approaches to improve them are suggested.

As described in Chapter I, the recent research areas of integrated optoelectronics are classified into the optoelectronic integrated circuit (OEIC), the photonic integrated circuit (PIC), and the optoelectronic integrated device (OEID). The monolithic photoreceiver described in Chapter IV belongs to the OEIC. The OEIC photoreceiver will be a key device in fiber-optic subscriber systems if further cost reduction is attained. It will be applied to large capacity transmissions if the inherent merit in high-speed operation is fully exhibited.

The IPC laser described in Chapter III is considered to be a basic component of PIC though it can be used as a solitary light source. In the proposal of PIC, active devices such as lasers, modulators, optical switches, and photodetectors are connected with passive waveguides. The PIC can be applied to wavelength division multiplexing (WDM) and coherent transmissions. In the future, electronic circuits will also be integrated in the PIC,

which is thought to be the unification of PIC and OEIC.

The PPM described in Chapter V is the OEID based on the new concept, that is, a two-dimensional array of conventional OEID's. The array-type OEID will be applied to optical interconnections and optical computing. As a combination of OEID and OEIC, a two-dimensional array of OEIC's can be constructed. The optically erasable PPM may be recognized as this type since the unit cell of OE-PPM form a circuit. The future optical signal processings based on integrated optoelectronics will be realized through the combination or unification of OEIC, PIC, and OEID.

As described above, all of the devices demonstrated in this study can be applied independently to some systems, and the unification of them will reach the final goal of optical signal processings. The author believes that they will be utilized soon in practical systems and unified finally into an optical signal processor by continuing research and development of the integrated optoelectronics.

—— **ADDENDUM** ——

I. LIST OF PUBLICATIONS

1-1. Full-Length Papers

1) "High-Current InGaAsP-InP Phototransistors and Some Monolithic Optical Devices,"
A. Sasaki, K. Matsuda, Y. Kimura, and S. Fujita,
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2) "A Monolithically Integrated InGaAs/InP Photoreceiver Operating with a Single 5-V Power Supply,"
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3) "Approach to High Speed Operation of InGaAs/InP Monolithic PIN/Amplifier,"
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1-2. Letters

1) "Cd-doping in $In_xGa_{1-x}As_yP_{1-y}$ Mixed Semiconductors Grown by Liquid-Phase Epitaxy,"
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T. Fujita, J. Ohya, K. Matsuda, M. Ishino, H. Sato, and H. Serizawa,
Electron. Lett., vol. 21, pp. 374-376, Apr. 1985.

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K. Matsuda, H. Adachi, T. Chino, and J. Shibata,
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1-3. Conference Proceedings

1) "Photonic Parallel Memory,"
K. Matsuda, J. Shibata, and T. Kajiwara,
Proc. International Topical Meeting on Photonic Switching, Kobe, 1990; K. Tada and H.S. Hinton, Eds., Springer Series in Electronics and Photonics, vol. 29: Photonic Switching II, Berlin, Heidelberg: Springer-Verlag, 1990, pp. 159-166.

2) "Optoelectronic Approach to Optical Parallel Processing Based on the Photonic Parallel Memory (PPM),"
K. Matsuda and J. Shibata,
Proc. SPIE's International Symposium on Optical Applied Science and Engineering, San Diego, 1991; D.M. Gookin, Ed., SPIE Proceedings, vol. 1562: Devices for Optical Processing, Bellingham, WA: SPIE, 1991.

II. LIST OF PRESENTATIONS

2-1. International Conferences

1) "A Monolithically Integrated InGaAs/InP Photoreceiver Operating with a Single 5 V Power Supply,"
K. Matsuda, M. Kubo, K. Ohnaka, and J. Shibata,
13th European Conference on Optical Communication (ECOC '87), Helsinki, 1987, Tech. Dig. vol. I, p. 39.

2) "1 Kbit InGaAsP/InP Optoelectronic Memory with a Function of Optical Parallel Processing,"
K. Matsuda, K. Takimoto, J. Shibata, and T. Kajiwara,
Seventh International Conference on Integrated Optics and Optical Fiber Communication (IOOC '89), Kobe, 1989, paper 20C3-2.

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5) "256 bit Parallel XOR Gate Operating with Optical Input and Output,"
K. Matsuda, H. Adachi, T. Chino, and J. Shibata,
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6) "Optoelectronic Approach to Optical Parallel Processing Based on the Photonic Parallel Memory (PPM),"
K. Matsuda and J. Shibata,
SPIE's International Symposium on Optical Applied Science and Engineering, San Diego, 1991, paper 1562-03 (invited).

2-2. Domestic Conferences

2-2-1. Institution of Electronics, Information and Communication Engineers (IEICE)

1) "Narrow Spectral Linewidth Characteristics of Monolithically Integrated Passive Cavity InGaAsP/InP Semiconductor Laser,"
T. Fujita, J. Ohya, K. Matsuda, H. Sato, and H. Serizawa,
National Convention, Kanagawa Univ., 1985, paper 898.

2) "OEIC Photoreceiver Using InP System,"
K. Matsuda, M. Kubo, K. Ohnaka, and J. Shibata,
Technical Group Meeting on Opto-Quantum Electronics, Tokyo, 1986, paper OQE86-68.

3) "InGaAs/InP Monolithic PIN/Amplifier Photoreceiver,"
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K. Matsuda, K. Takimoto, and J. Shibata,
Spring National Convention, Kinki Univ., 1989, paper C-412.

5) "An Optically Erasable Photonic Parallel Memory,"
H. Adachi, K. Matsuda, T. Chino, and J. Shibata,
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2-2-2. Japan Society of Applied Physics (JSAP)

1) "Electrical Characteristics of Cd-doped p-type InGaAsP,"
K. Matsuda, S. Fujita, and A. Sasaki
42th Autumn Meeting, Fukui Univ., 1981, paper 7p-U-8.

2) "Fabrication and Characterization of High-Current InGaAsP/InP Phototransistors,"

K. Matsuda, M. Taneya, S. Fujita, and A. Sasaki,
29th Spring Meeting, Tokyo Science Univ., 1982, paper 2a-R-2.

3) "Light Amplification and Wavelength Conversion by Using InGaAsP/InP Phototransistors,"
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5) "Ohmic Contact on p-type InGaAsP,"
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6) "InGaAsP/InP Monolithic External Cavity Lasers (I) : Fabrication,"
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7) "InGaAsP/InP Monolithic External Cavity Lasers (II) : Static Characteristics,"
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9) "Dependence of Spectral Linewidth on Cavity Length for InGaAsP Monolithic External Cavity Lasers,"
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46th Autumn Meeting, Kyoto Univ., 1985, paper 1p-M-7.

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37th Spring Meeting, Toyo Univ., 1990, paper 30p-F-13.