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Photonic Parallel Memory

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1. Introduction

There has been much interest in integration of optical or optoelectronic bistable switches because of its capability of application to optical interconnection and parallel processing. As for a single bistable switch, various kinds of devices have been proposed and demonstrated, such as a Fabry-Perot etalon with a nonlinear optical material[1], a laser amplifier[2], a laser diode with saturable absorber[3], a self electro-optic effect device (SEED)[4], an LED with pnpn or pnn structure[5,6], and an integrated device of a phototransistor with a laser diode or a light emitting diode (LED)[7-10]. Among them, the switch consisting of LED and a heterostructure phototransistor (HPT) has advantages of inherent gain and unidirectionality for optical signals[9] as well as simple structure suitable for large scale integration[10].

An integrated device of LED and HPT was first proposed by A. Sasaki et al. for application to light amplification[11]. This device shows bistability in both voltage-current and optical input-output characteristics because of optical positive feedback from LED to HPT unless the feedback is intentionally suppressed[6]. In this paper we demonstrate an array of 32 x 32 bistable switches consisting of LED and HPT. This photonic parallel memory (PPM) can be written in and read out with 1 Kbit parallel optical signals. It can operate also as a 1 Kbit parallel OR gate when different signals are written in either sequentially or simultaneously. Considering the array operation, it is important to decrease both the dissipation current for a single switch and the input optical power necessary to turn on the switch. These values

have been measured for switches with different device parameters. The switching speed has also been evaluated.

2. Structure

The structure of PPM is shown in Fig. 1. It contains 32 X 32 mesas isolated by etched grooves. The groove has a width of 4 μm and a depth of 5 μm, and the remained mesa has an area of 16 X 16 μm^2. Each mesa is the bistable switch consisting of seven layers which are an n-InP emitter ($\sim$ 2 μm, 5 X 10^{17} cm^{-3}), a p-InGaAsP base (0.25 μm, 1 X 10^{17} cm^{-3}, bandgap wavelength λ_g=1.3 μm), an n-InP collector (0.9 μm, 1 X 10^{17} cm^{-3}), an n-InP clad (0.9 μm, 1 X 10^{18} cm^{-3}), an InGaAsP active layer (0.3 μm, undoped, λ_g=1.3 μm), a p-InP clad (1.0 μm, 5 X 10^{17} cm^{-3}), and a p-InGaAsP cap (0.1 μm, 2 X 10^{18} cm^{-3}, λ_g=1.1 um). The first three and the rest four layers constitute HPT and LED, respectively. All the switches are wired in parallel with a Ti/Au interconnection metal. The Ti/Au play also a role of optical isolation for the switches since it surrounds all the side walls of the mesas. The fabricated chip is shown in Fig. 2. The chip has an area of 1.0 X 1.0 mm^2 including bonding pads and single switches for testing, while the active area for integration is 640 X 640 μm^2.

3. Characteristics

An example of voltage-current characteristics for a single switch are shown in Fig. 3. As shown in (a), a thyristor-like voltage-current curve was observed unless input light was incident. As input optical power was increased, the breakdown voltage was decreased and a diode-like curve shown in Fig. 3(b) was observed when the input power was 175 μW. In case of operating it with a constant bias voltage, the switch is turned on before this condition. In other words, the input optical power necessary to turn on the switch (switch-on power) depends on the bias voltage and the maximum value is equal to the input optical power necessary to obtain diode-like curve. The experimental setup for operating PPM is shown in Fig. 4 together with the schematic diagram of memory operation. An example of memorized

pattern on a PPM chip observed with an infrared video camera is shown in Fig. 5. A Chinese character is displayed with 56 selected switches which are turned on and emit light.

The minimum current to maintain the on-state (holding current) can be found from voltage-current characteristics and is 1.6 mA for the switch shown in Fig. 3. The characteristics for another switch with a holding current of 600 μA are shown in Fig. 6. The input optical power necessary to obtain diode-like curve has also been reduced to be 20 μW. For this switch, the collector of HPT was changed to be InGaAsP and the base was made to be thinner (~0.15 μm). To separate the cause for reduction of holding current, the relations between breakdown voltage without input light and holding current have been measured for three types of switches which were selected from three different wafers. They are the wafer with an InP collector and a thick (~0.25 μm) base (#31), with a quarternary collector and a thick base (#33), and with a quarternary collector and a thin (~0.15 μm) base (#35). The results are shown in Fig. 7. The breakdown voltage depends on the thickness of the base layer and the various values of breakdown voltage observed in switches on the same wafer is attributed to non-uniformity of layer thickness.

To evaluate the switching speed of PPM, the optical pulses with various pulse width were incident upon one of the integrated switches and switch-on power were measured. The results are shown in Fig. 8. The measurement was done for three types of PPM chips on wafers #31, #33, and #35 mentioned in the previous section. The light pulse with a width of 5 ns can turn on the switches on wafers #33 and #35 though the switch-on power is increased as the pulse width is decreased. The product of switch-on power and pulse width for short pulse region is calculated to be 1.2 pJ for the switch on #35.

4. Discussion

The dissipation current (I_d), the output optical power (P_{out}), and the input optical power (P_{in}) of the switch are related by following equations

$$P_{out} = \eta_e I_d \quad (1)$$

$$I_d = G (kP_{out} + P_{in}) \quad (2)$$

where η_e is the efficiency of LED in W/A, G is the optical gain of HPT in A/W, and k is the optical coupling efficiency between LED and HPT. In the case of $P_{in} = 0$, the trivial solution of Eqs. (1) and (2) is $I_d = 0$, which denotes the off-state. The other solution corresponding to the on-state is $G(I_d) = (k \eta_e)^{-1}$. Therefore, it is important to fabricate HPT with high optical gain in low current region in order to obtain the switch with low dissipation current. As can be seen from Eq. (2), such HPT can also reduce the minimum input optical power to turn on the switch. The above discussion can qualitatively explain the experimental results shown in Fig. 7. The optical gain of HPT is the product of optical absorption efficiency (η_a) and current gain (β). The switches with a quarternary collector have smaller holding current than those with an InP collector because the quarternary collector increases η_a. The switches with a thinner base have smaller holding current since it increases β.

5. Conclusions

1 Kbit PPM which is an array of 32 X 32 optoelectronic bistable switches has been fabricated successfully. The memory operation of PPM with functions of optical write-in and read-out has been demonstrated. The minimum current to maintain the on-state and the input optical power necessary to turn on the switch were improved to be 600 μA and 20 μW by using a quarternary collector and a thin base. The light pulse with a width of 5 ns was able to turn on the switch and the product of switch-on power and pulse width for short pulse region was 1.2 pJ.

References

[1] H.M. Gibbs, S.L. McCall, T.N.C. Venkatesan, A.C. Gossard, A. Passner, and W. Wiegmann, Appl. Phys. Lett. **35**, 451 (1979).

[2] T. Nakai, N. Ogasawara, and R. Ito, Japan. J. Appl. Phys. **22**, L310 (1983).

[3] H. Kawaguchi and G. Iwane, Electron. Lett. **17**, 167 (1981).
[4] D.A.B. Miller, D.S. Chemla, T.C. Damen, T.H. Wood, C.A. Burrus, Jr., A.C. Gossard, and W. Wiegmann, IEEE J. Quantum Electron. **QE-21**, 1462 (1985).
[5] T. Inoguchi, T. Sakurai, Z. Tani, Z. Shigemasa, and T. Mori, Sharp Tech. J. **8** (2), 13 (1969).
[6] G.W. Taylor, J.G. Simmons, A.Y. Cho, and R.S. Mand, J. Appl. Phys. **59**, 596 (1986).
[7] Y. Ogawa, H. Ito, and H. Inaba, Japan. J. Appl. Phys. **20**, L646 (1981).
[8] A. Sasaki, K. Matsuda, Y. Kimura, and S. Fujita, IEEE Trans. Electron Devices **ED-29**, 1382 (1982).
[9] A. Sasaki, M. Taneya, H. Yano, and S. Fujita, IEEE Trans. Electron Devices **ED-31**, 805 (1984).
[10] K. Matsuda, K. Takimoto, J. Shibata, and T. Kajiwara, in Technical Digest, Seventh International Conference on Integrated Optics and Optical Fiber Communication (Kobe, 1989), paper 20C3-2.
[11] A. Sasaki and M. Kuzuhara, Japan. J. Appl. Phys. **20**, L283 (1981).

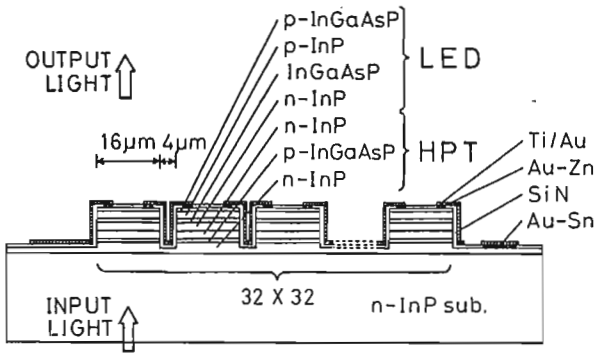

Fig. 1 Schematic cross section of PPM. Each mesa consisting of LED and HPT is a bistable switch.

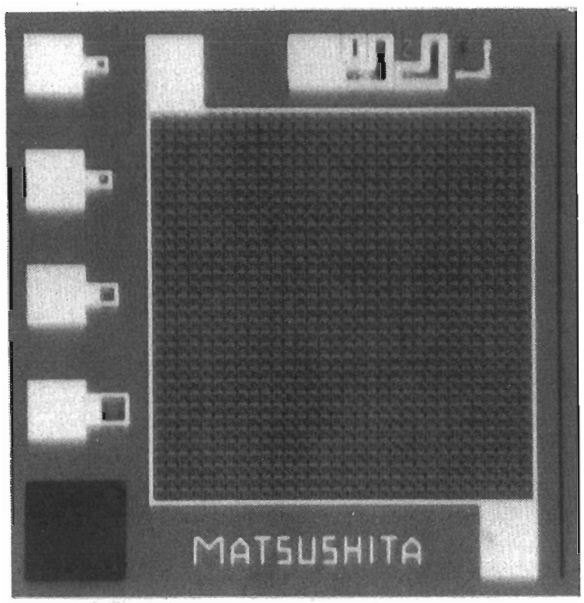

Fig. 2 Photomicrograph of a fabricated PPM chip. The chip size is 1.0 X 1.0 mm^2 including bonding pads and single switches for testing.

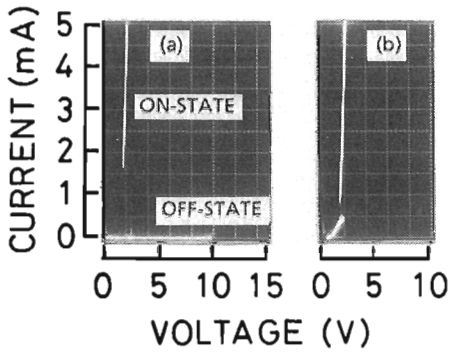

Fig. 3 Voltage-current characteristics of a single switch with an InP collector and a thick (~ 0.25 μm) base: (a) without input light and (b) with an input light of 175 μW.

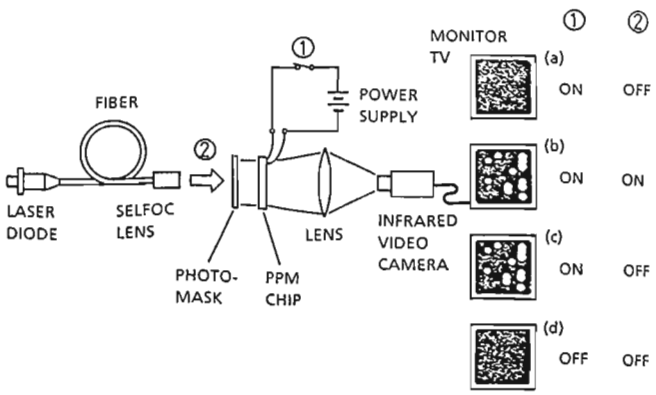

Fig. 4 Experimental setup for operating a PPM chip together with the schematic diagram of memory operation: (a) initial state, (b) write-in, (c) memory, and (d) reset.

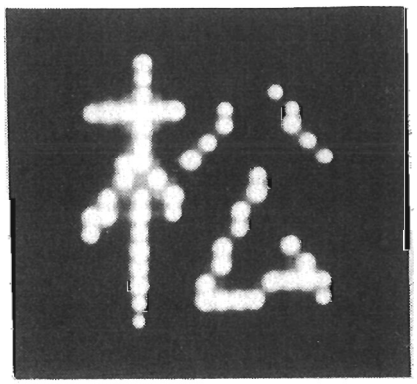

Fig. 5 Infrared image of a PPM chip in memory operation. A Chinese character meaning "a pine tree" is memorized and read out.

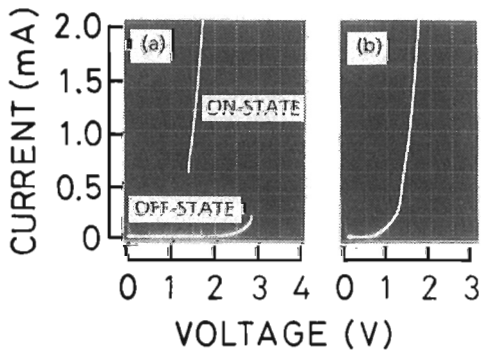

Fig. 6 Voltage-current characteristics of a single switch with a quarternary collector and a thin (~ 0.15 μm) base: (a) without input light and (b) with an input light of 20 μW.

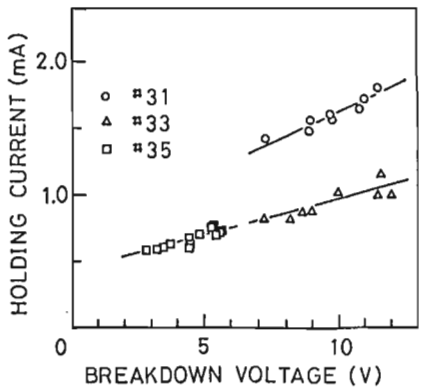

Fig. 7 Relations between breakdown voltage and holding current: with collector/base of InP/thick (#31), quarternary/thick (#33), and quarternary/thin (#35).

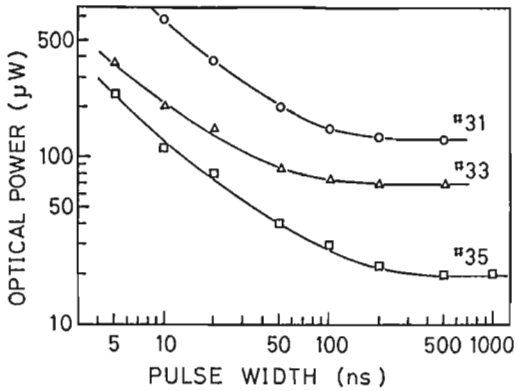

Fig. 8 Relation between pulse width of input light and switch-on power for single switches integrated in PPM chips on wafers #31, #33, and #35.