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Photonic Parallel Devices with Memory and Logic Functions

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I. Introduction

Conventional computers based on VLSI technologies suffer from communication problems such as interconnection bandwidth, clock skew, and von Neumann bottleneck. These problems will be overcome by using optical signals for interconnections since light has inherent advantages of large bandwidth, dense parallel transmission, and non-interfering propagation. In application of optics or photonics to computer systems, three possibilities can be considered. One is combination of electronic processing and optical interconnections. In this case, optical signals are used only for interconnects while logic gates and memories are constructed with electronic devices. Although it is the most realistic way, the optical interconnection is insufficient to maximize the merits of optical signals. The second approach is optical computing in which signal processing itself is done by optics. The "pure" optical computing has potential of ultra-high speed operation though it usually needs high optical power. This is attributed to the difficulties in interacting two streams of photons that is the very reason why optical beams are suitable for interconnections.

The third is optoelectronic approach where optoelectronic devices with logic and memory functions are utilized for signal processing. Though the speed of optoelectronic devices is limited by electrons, the logic and memory functions can easily be obtained by the assistance of electronics. If thousands or millions of optoelectronic functional devices are integrated in a two-dimensional array, the direct image processing much faster than the sequential pixel-by-pixel processing will be achieved. Such an array can be defined as a new type of optoelectronic integrated circuit (OEIC) [1]. In this paper, we demonstrate such an OEIC named a photonic parallel memory (PPM) and its advanced model. The PPM is an array of the optoelectronic bistable switches each of which consists of a light emitting diode (LED) and a heterojunction phototransistor (HPT). The PPM can be used not only as a memory but also as a logic gate. In the advanced model, the LED and the HPT are replaced by a surface emitting laser (SEL) and a heterojunction bipolar transistor (HBT), respectively, for higher-speed operation.

II. PPM based on LED/HPT stacked devices

The PPM developed for the first time was a 1 Kbit PPM in which 32 X 32 optoelectronic bistable switches were integrated [2]. Its structure is shown in Fig. 1(a). Each mesa isolated by etched grooves is a bistable switch consisting of an LED and an HPT. The stacked device of the

LED and the HPT were originally proposed by Prof. A. Sasaki of Kyoto University for application to light amplification [3]. In the stacked device, input light is detected by the HPT, and the photocurrent of the HPT directly drives the LED to emit output light. Since this input-to-output conversion includes transistor gain, light amplification can be achieved. Furthermore, optical bistability is obtained in case that a part of the light emitted from the LED is fed back to the HPT. The optoelectronic bistable switch integrated in the PPM is the LED/HPT stacked device with a strong feedback. Once the input light is incident upon the switch, the light emission is maintained after removing the input light. Light emission from a PPM chip displaying a memorized pattern is shown in Fig. 2.

The 1 Kbit PPM is written-in and read-out by optical signals though erasing is done by decreasing the bias voltage. In the second step of development, an optically erasable (OE-) PPM was fabricated [4]. To attain the optical reset, an additional HPT and a load resistor are integrated in the unit cell of the OE-PPM. The structure of the unit cell is shown in Fig.1(b). It contains two mesas which correspond to a bistable switch and a reset HPT. When set light is incident upon the switch, the switch is turned on. In case that reset light is put into the reset HPT, the current through reset HPT increases the voltage drop in the load resistor, and the switch is turned off. Differently from the reset operation by controlling the bias voltage, this reset operation is selective, that is, only the selected switches are turned off. The bistable switch has a logic function of the OR gate since an output signal of A OR B is obtained for input signals A and B. The optical reset function realizes the NOT gate. As a result, all the logic functions can be attained by the OE-PPM [5].

The OE-PPM has two inputs and one output. To obtain symmetric input-output configuration, two types of PPMs have been developed. The first one is a differential output (DO-) PPM having two inputs and two outputs [6]. Its structure is shown in Fig. 1(c). The DO-PPM contains two optical inverters each of which consists of a parallel connection of an LED and an HPT with a load resistor connected in series to them. In the optical inverter, the LED stops emitting output light when input light is incident upon the HPT. Since two optical inverters are coupled optically, the differential operation similar to an electronic RS flip-flop is performed. The second one is a dynamic reset (DR-) PPM having one input and one output [7]. As shown in Fig. 1(d), it has a stacked structure of an LED and two HPTs. The LED and one of the HPTs are connected electrically in series to form a bistable switch. The other HPT is connected in parallel to the switch for reset operation. A single optical beam modulated with pulse signals is input to both HPTs simultaneously. The optical pulse with a peak power in some range turns on the switch, and the pulse with a higher peak power turns off it as demonstrated in Fig. 3.

III. 2-D Array of SEL/HBT stacked devices

In general, the LED and the HPT are not suitable for high speed operation. By replacing them to an SEL with a vertical cavity and an HBT with a base contact, higher speed operation can

be expected. Since the SEL emits output light vertically to the surface, the same stacked structure as the LED/HPT-based PPMs can be constructed. In the first step of development, an array of SEL/HBTs without optical feedback has been fabricated [8]. This SEL/HBT has a linear gain and driven by electrical inputs. The structure and the equivalent circuit are shown in Fig. 4. The HBT is set on the SEL so that the emitter size of the HBT can be reduced regardless of the SEL size. The SEL has a conventional structure of an InGaAs/GaAs quantum well sandwiched by GaAs/AlAs distributed Bragg reflectors (DBRs) though the bottom DBR is of p-type. This common-anode configuration has another advantage that the resistance caused by an abrupt interface between p-type GaAs and AlAs can be reduced because the current flows through the p-DBR with a large area [9]. The HBT has no collector contact since the collector layer is directly connected to the n-type DBR of the SEL. The row and column interconnections for the bases and the emitters are formed on a planar surface covered with polyimide.

An HBT in the SEL/HBT array is operated as shown in Fig. 5. A current gain over 40 is obtained. Since the collector is connected to the external circuit through the SEL, the collector-emitter voltage includes the voltage drop in the SEL. Gradual increase of current in the saturation region is due to the resistance of the p-type DBR. Output optical power of the SEL/HBT in relation to the collector and the base current is shown in Fig. 6 with open squares and closed circles, respectively. The former shows the current-light characteristics of the SEL. A threshold current of 3.5 mA is obtained. The latter emphasizes the smaller current can drive the SEL when the modulation signal is input to the base. An output power of 10 μW is emitted at zero base current since the breakdown leakage current flows through the collector at the applied bias voltage of 13 V. The resistance of the p-type DBR can be reduced by increasing the doping level in the upper layers of the DBR, which has already been verified for a solitary SEL [10].

In the SEL/HBT described above, the HBT is utilized only as an electronic device. This is because the light emitted from the SEL with a lasing wavelength of 0.98 μm is not detected by the HBT having a GaAs base. The HBT with an InGaAs base is required to detect the SEL output. By using a compositional graded layer, the HBT with an InGaAs base can be grown on the GaAs substrate. After such an HBT is fabricated successfully, it will be possible to construct the PPMs based on the SEL/HBT.

IV. Conclusions

The PPMs based on the LED/HPT stacked devices have been demonstrated. The OE-PPM is written-in, read-out, and erasing by optical parallel signals. The DO-PPM operates in the same manner as an electronic RS flip-flop. The DR-PPM is set and reset by a single optical beam. The SEL/HBT array has been fabricated for higher speed operation where the LED and the HPT are replaced by an SEL and an HBT, respectively. The modulation current of the SEL is successfully reduced by integrating the HBT. The PPMs based on the SEL/HBT will be realized in the near future.

References

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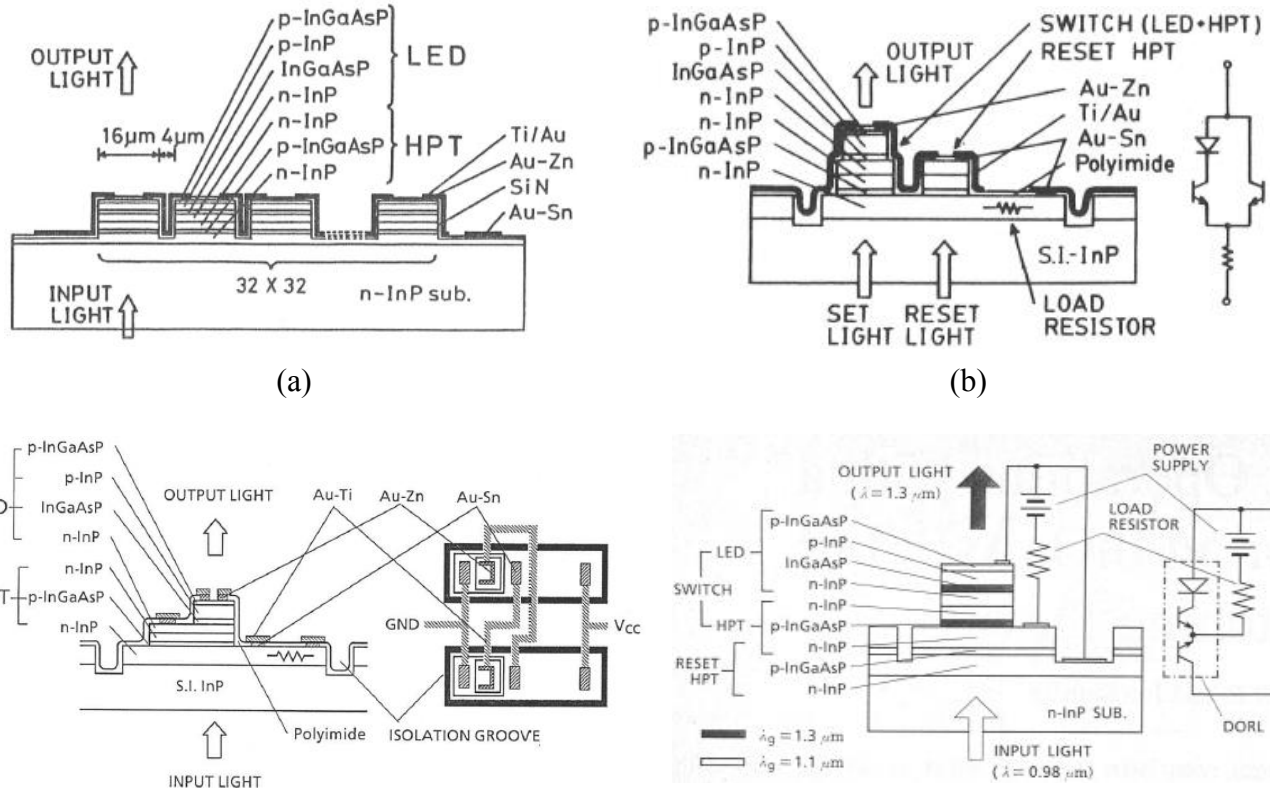

Fig.1 Structures of various types of photonic parallel memories (PPMs): (a) 1 Kbit PPM, (b) optically erasable (OE-) PPM, (c) differential output (DO-) PPM, and (d) dynamic reset (DR-) PPM.

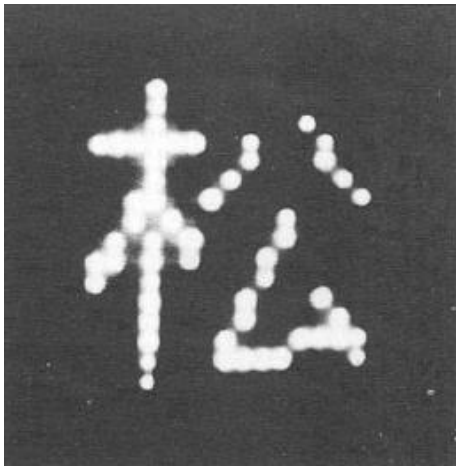

Fig. 2 Infrared image of a PPM chip in memory operation. A Chinese character "MATSU" is displayed.

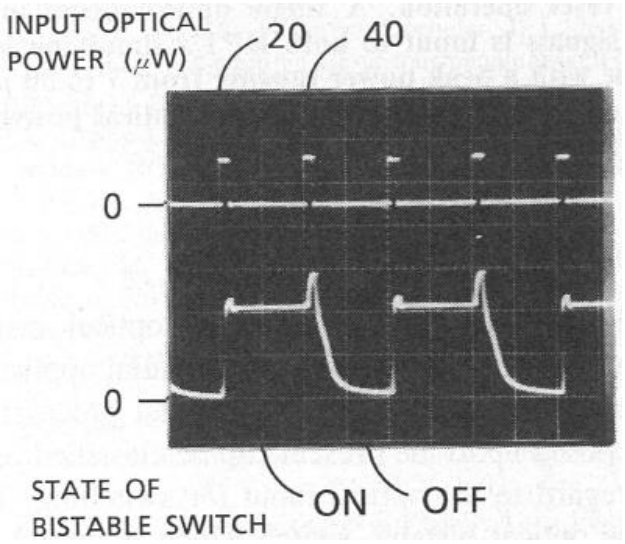

Fig. 3 Oscilloscope traces of dynamic set and reset operations. The upper trace shows the driving voltage for a light source. The lower is voltage drop through the load resistor.

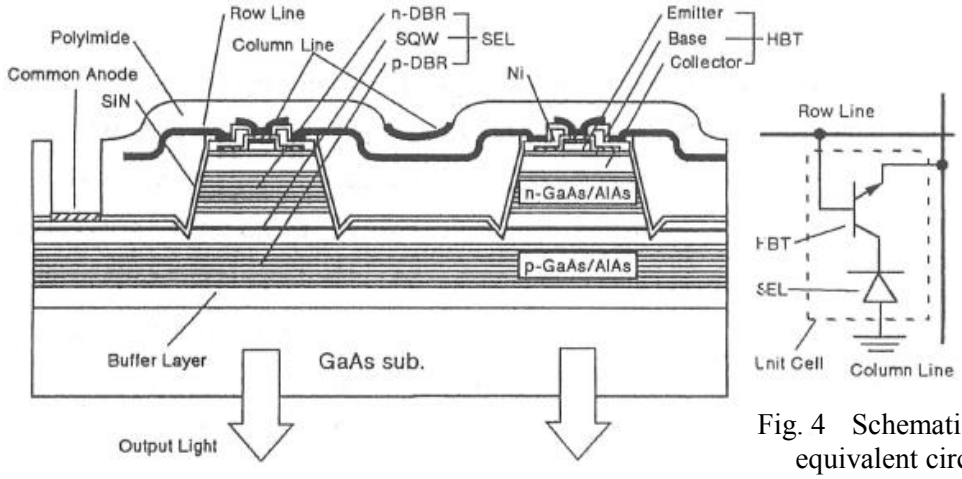

Fig. 4 Schematic cross section and equivalent circuit of the SEL/HBT array.

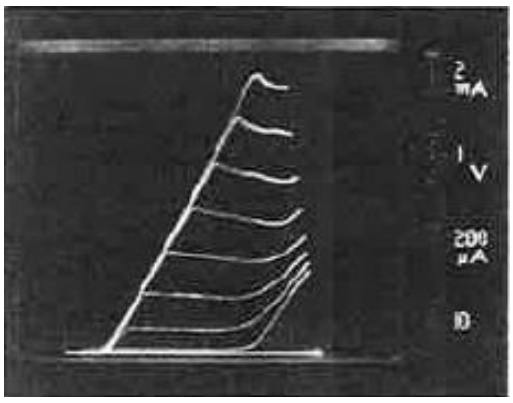

Fig. 5 Voltage-current characteristics of an HBT in the SEL/HBT array.

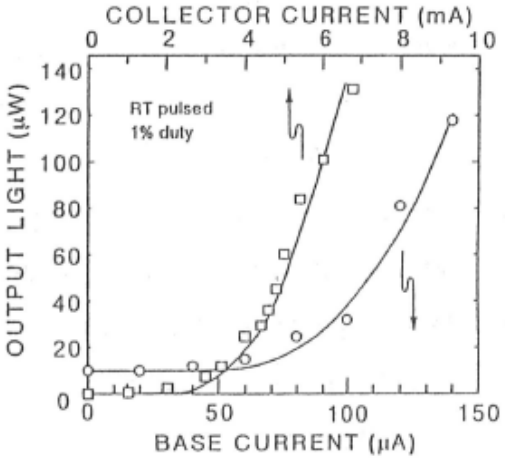

Fig. 6 Output optical power in relation to the collector and the base current.